Analysis of Various Domino Logic Designs for Low Power Consumption, Noise Immunity and High Speed Performance

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Abstract: *Performance of domino logic circuits is degraded by technology scaling due to exponential increase in leakage. Here various domino logic designs circuits are reviewed to improve the performance. Lower power consumption is achieved from comparative analysis of various domino circuits. Lower leakage and higher noise immunity has been achieved without speed degradation for wide fan-in gates. In CCD technique, contention current, consequently power consumption and delay are reduced. Simulation results in 16-nm high-performance predictive technology model demonstrate 51% power reduction and at least 2.41 X noise-immunity improvement at the same delay compared to the standard domino circuits for 64-bit OR gates. Replacement of bulk CMOS through FinFET devices show 2.7 times less power consumption.*

Keywords: *Domino logic, FinFET, High-speed, Low Power & High noise immunity*

1. INTRODUCTION:

DOMINO logic is a CMOS based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. DL circuits allows rail to rail logic swing and was developed to speed up circuits. Domino logic or dynamic logic is widely used in applications to achieve high performance which cannot be achieved by static logic. More sensitive to noise is the main drawbacks of DL circuits. High performance critical units of microprocessors uses high fan in compact dynamic gates which is strongly affected by subthreshold leakage and noise sources. Because in scaled technologies leakage current is exponentially increased due to decreased threshold voltage. In technology scaling supply voltage scaling is used to reduce power consumption. In domino circuits less threshold means smaller gate switching trip point which makes the domino circuits more prone to input noise. Moreover due to excessive leakage the precharge (dynamic) node of a domino circuit can discharge resulting in a logic failure (wrong evaluation). If we reduce trip point and increased leakage the other noise sources such as supply noise and cross talk noise also increase by technology scaling which degrade the robustness of domino logic.

Improving noise immunity and reduction of leakage current are of major concern in robust and high performance designs, especially in wide fan-in dynamic gates employed in the read path of registers files, L1 caches, Flash memories, tag comparators, programmable logic arrays, wide multiplexer-flip-flop(MUX) and De-MUX. In this paper, various performance-comparison-based domino circuits are reviewed.

2. LITERATURE REVIEW:

A conventional approach to improve the robustness is the conventional standard domino circuit as shown in fig. 1. Proposed by [2] which employ pMOS keeper transistor. In this design, any undesirable discharging at the dynamic node is prevented due to the leakage current and charge sharing of pull-down network(PDN) during the evaluation phase. Hence improve the robustness. The keeper ratio KR is defined as

$$\boldsymbol{KR} = \frac{\mu_p\left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n\left(\frac{W}{L}\right)_{evaluation-network}} \qquad (1)$$

Where W and L denote transistor size and μ_p and μ_n are electro and hole mobilities.

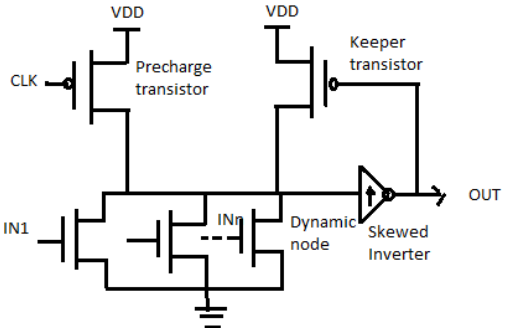

Fig. 1. SFLD design

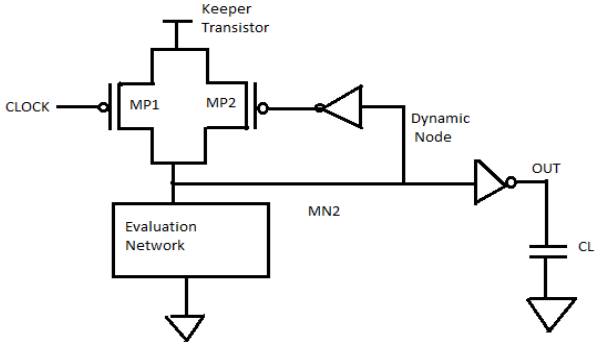

Fig.2.Footless Domino Logic Circuit(FLDL)

The keeper transistor upsizing improves noise immunity and increases current contention between the keeper transistor and evaluation network even then in the new scenario of CMOS technology it is less effective. Moreover current contention increases evaluation delay and power consumption of the circuit. These problems are of critical issue.

However keeper upsizing trade off delay and power to improve noise and leakage immunity but trade off is not acceptable because it make the circuit too slow and power consumable.

Hence various techniques are reviewed to address above issues. Successive improvement is studied in further sections such as section 2 explains conventional domino logic style, section 3 explain high performance circuit for high fan in applications, section 4 shows simulation result and section 5 conclusion are drawn.

3. Domino logic style:

Domino logic styles include footless standard domino logic (FLDL), footed standard domino logic (FDL), high domino logic (HSDL) and conditional keeper logic (CKL) proposed by [1]

3.1 Footless standard domino logic (FLDL)

Primarily, domino logic is designed for high speed applications but sensitivity of the dynamic node is too much prone to the noise sources in scaled technologies. Moreover keeper transistor is added to provide immunity to noise and leakage for the dynamic node. Schematic design of footless domino logic is shown in fig. 2. Proposed by [1] Addition of PMOS keeper transistor degrades performance and increases power dissipation in the circuit. Keeper transistor upsizing increases contention between the keeper transistor and evaluation network. Therefore small size keeper is desirable for high speed application while large keeper is required for robust design.

When a noise pulse is applied to the input of the circuit, it fails to operate correctly. This is due to the large amount of leakage for short channel devices. Hence leakage current is a savvier issue in FLDL.

3.2 Footed domino logic circuit (FDL)

To overcome the problem of FLDL a footer NMOS transistor is connected to the sources of evaluation NMOS transistor shown in fig. 3. This technique reduces the leakage power significantly but degradation in the speed of operation. Further, robust operation is not shown in FDL [3] for wider gates. Hence several techniques are discussed to improve leakage and power consumption in domino logic circuits.

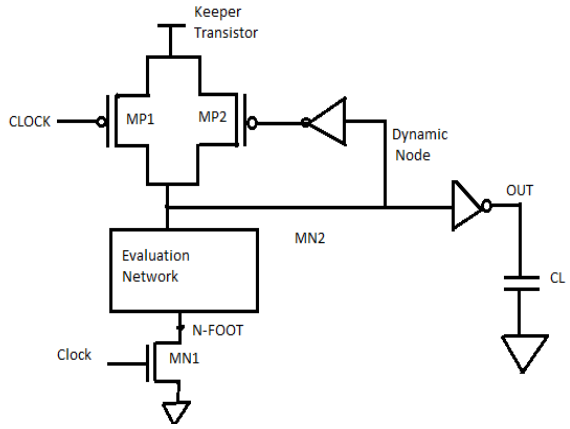

Fig. 3.Footed Domino Logic (FDL)

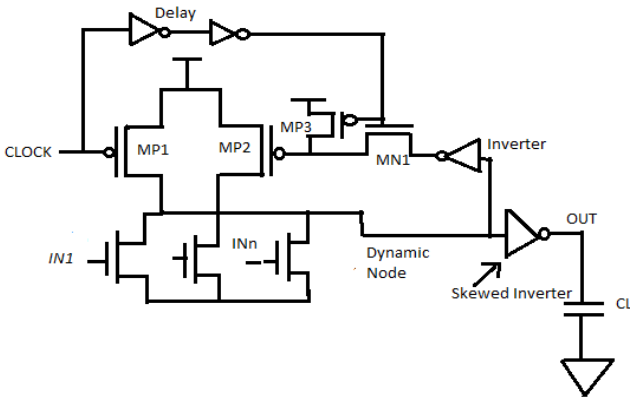

Fig. 4. High Speed Domino Logic (HSDL)

3.3 High speed domino logic (HSDL)

The circuit topology is shown in fig. 4. At the beginning of the evaluation phase, when clock is high, MP3 turns ON and then the keeper transistor MP2 turns OFF. Due to this contention between evaluation network and keeper transistor is reduced. When delay of the transistor equals the delay of the two inverter ($2\times T_{inv}$), transistor MP3 turns off. If the dynamic node is discharged to ground, the NMOS transistor MN1 remains OFF. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at"0", standby mode), MN1 pulls the gate of the keeper transistor to zero and turns on the keeper transistor to keep the dynamic node high. In case of large noise at inputs, the evaluation network network discharges the dynamic node causing the failure at the output of the circuit. Increased power dissipation s the another drawback of this design.

3.4 Conditional keeper logic (CKL)

The schematic circuits of the conditional keeper logic is shown in fig. 5. At the beginning of the evaluation phase, the smaller keeper(K1) turns ON to keep the state of the dynamic node. After the delay equals the delay of two inverters dynamic node is still high, the output of the NAND gate goes low and turns on the transistor K2. In order to improve the robustness of the circuit transistor K2 must be kept larger sized. Limitation on decreasing delays of the inverters are the drawbacks of this design.

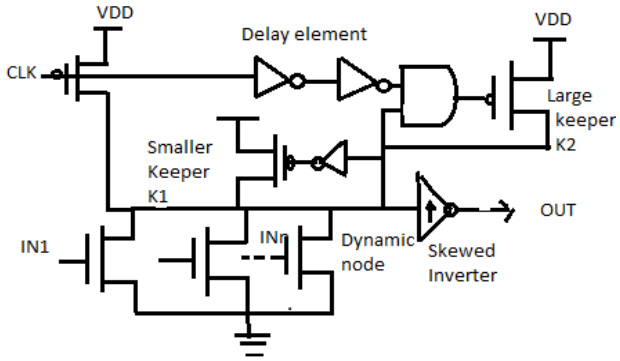

Fig. 5.Conditional keeper logic (CKL)

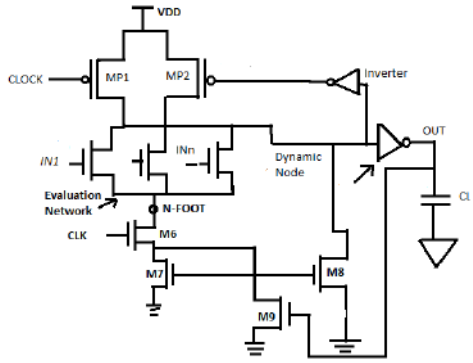

Fig.6. Current Mirror Footed Domino Logic (CMFDL)

4. High performance circuit for high fan in applications consist of various designs such as current mirror footed domino logic (CMFDL), High speed clocked –delayed domino logic style (HSCD), Modified HSCD (MHSCD), Conditional evaluation domino logic (CEDL), Conditional stacked keeper domino logic(CSKDL).

4.1. Current mirror footed domino logic (CMFDL)

In this design shown in fig. 6, transistor (M7) is connected to provide stacking effect in order to reduce leakage current during the evaluation phase. To reduce the evaluation delay of the transistor stack transistor (M8) is connected in parallel with the evaluation network to increase the discharging current. Transistor (M9) is connected between output and gate of current mirror and then to the ground when a dynamic node is discharged to ground. Transistor (M9) turns off current mirror when noise is present at the input and stops discharging the dynamic node. However, there is a trade-off between sizing of the mirror transistor and noise immunity.

When the clock is low, the circuit is in the discharge mode and the dynamic node gets precharged to high. When the footer transistor (M6) is turned off a very small leakage current passes through M7 pulling a negligible current from the dynamic node. In the evaluation phase when the clock is high the circuit shows significantly improved noise immunity due to the stacking effect provided by the transistor (M7). When the clock is high, if all the inputs are zero. These three stacks NMOS transistors (Meval-M6-M7)substantially reduces the threshold current. However, when at least one of the inputs switches to high, the mirror transistor-pulls large current from the dynamic node resulting in a high to low transition on the dynamic node.

In this case output of the gate goes high, turning on the NMOS transistor(M9) disabling the current mirror. For the rest of evaluation phase current mirror remains OFF, although a very high level of noise is applied to the inputs of evaluation phase. Here minimum size keeper transistor is used to reduce the contention between evaluation network and keeper transistor.

4.2. High speed clock-delay domino logic style (HSCD)

In this designed circuit a footer transistor MN1 which employs stacking effect is connected to the tail of the evaluation NMOS tree in order to improve noise immunity. It also uses the steady state voltage of N-FOOT node at the beginning of evaluation phase to reduce leakage of the evaluation network.

Different mode of operation of this circuit

Precharge mode:

As shown in fig.7 when clock is low, the circuit is in the precharge phase. MP1 is turned on and the dynamic node is charged to VDD. Moreover PMOS keeper transistor (MP2) is turned ON helping the precharge.

At the beginning of the precharge phase MN1 is ON connecting the N-FOOT node to ground. Also node GMN2 is low and MN2 is OFF. After the delay equal to the delay of inverters, MN1 turns ofF, voltage of N-FOOT rises to an intermediate voltage level. The evaluation transistors are sized such that the DC voltage on GMN2 node does not exceed the threshold voltage of MN2 to avoid any possibility of short circuit current in the precharge phase. Therefore transistor MN2 chosen large to help the evaluation of the circuit.

All inputs at zero in evaluation:

NMOS footer transistor MN1 is OFF at the beginning of the evaluation phase which result in floated node N-FOOT reaches a DC value. Transistor MP3 turns ON when this DC exceeds $|V_{tn}\text{-MP3}|+V_{OUT}$ (2)

In this case, GMN2 node is charged to VN-FOOT, therefore

$$VGMN2 \geq Vtn\text{-}Mn2 \rightarrow MP3{:}ON \quad (3)$$

Hence, wrong evaluation occurs. To avoid any failure, transistors MN1,MN2,MN3 & MN4 are sized in such a way that equation 1 & 2 are not satisfied.

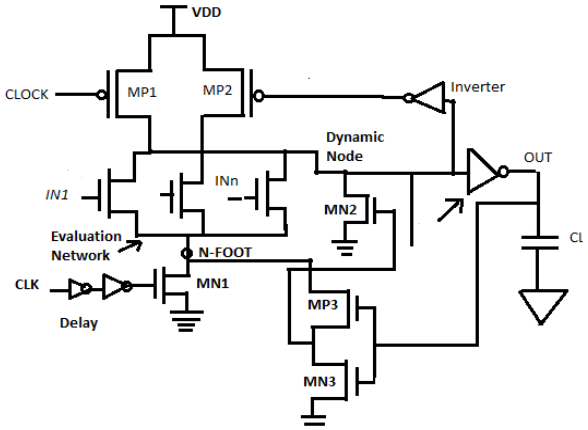

Fig. 7. High speed clock-delay domino logic

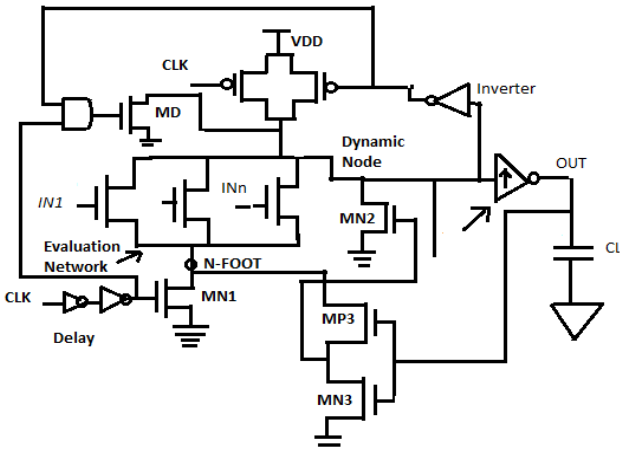

Fig. 8. Modified-HSCD

An input switching high

When transistor MP3 turns ON due to increased voltage on node N-FOOT at the beginning of the evaluation phase, node GMN2 is charged to a voltage and goes higher to the threshold voltage of MN2. The NMOS transistor MN2 turns on at the onset of evaluation phase. Amount of discharging current through MN2 depends on the sizing of MN2. After the delay equals the delay of two inverters, N-FOOT node is connected to ground and transistor MN3 switched OFF. When the dynamic node goes low, the output node becomes high, turning ON MN3 leads to turning OFF MN2

Here, we have all the options for improving speed, upsizing of MP3, MN2, MN1 and evaluation transistors. To improve the evaluation speed, an extra circuitry is used which is referred as Modified- HSCD (MHSCD) shown in fig. 8.

When at least one of the input is high, the dynamic node starts to discharge after the primary time of evaluation. Keeper transistor MP2 starts to go high, therefore both inputs of AND gate are high giving output of AND gate high. As a result transistor MD turns on and improves the speed of evaluation. In all other cases, output of the AND gate is “0” . Hence transistor MD is switched OFF.

The main drawbacks of this design is of increased power dissipation due to floating gate of of NMOS transistor MN2 during precharge node.

4.3. Conditional evaluation domino logic (CEDL)

In designed circuit shown in fig. 9, the stacked NMOS transistors MN2 & MN3 turn ON conditionally. For a delay equal to the delay of the two inverter, footer transistor remains OFF. This causes a voltage bump on N-FOOT node. By changing the size of the footer transistor and evaluation NMOS transistor this value get modulated. Upsizing the footer transistor and evaluation network transistor lowers the voltage on node N-FOOT and elevates N-FOOT voltage respectively. To illustrate this effect, the transistor sizes for parallel NMOS network are swept from 400nm to 1µm. The larger the NMOS transistors are, larger the value of N-FOOT voltage is. Upsizing the evaluation network NMOS transistors (W_{Eval}) rises the voltage value on node N-FOOT.

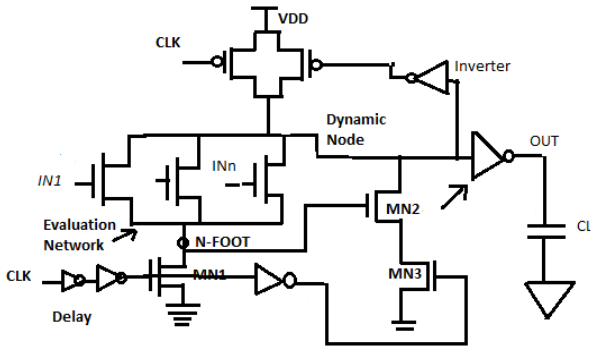

Fig.9. Conditional Evaluation Domino Logic (CEDL)

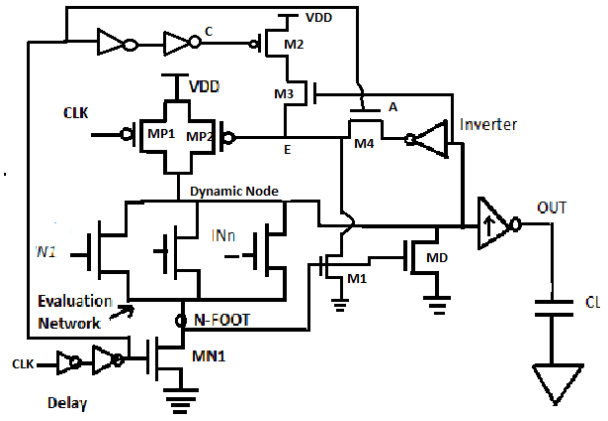

Fig. 10. Conditional stacked keeper domino logic (CSKL)

4.4. Conditional stacked keeper domino logic (CSKL)

In this design as shown in fig. 10. A feedback from a footer transistor to discharge the dynamic node when at least one input in evaluation network is "1". During evaluation, clock goes high, for a delay equal to the delay of two inverters, node A & C are "0". Hence, M2 and M3 turn ON while M4 turn OFF. At the same the time, assuming atleast one of the evaluation network input is "1". Depending on the sizing of the transistor, N-FOOT node is charged to a value greater than 0.4V due to which transistor M1 turns ON and dynamic node get discharge to ground. At this time, M1 turns ON which leads to a weaker MP2 transistor. Hence reduces the contention between MD and MP2. When node E holds a value higher than (V_{DD}-V_{TH}), transistor M1 helps to make MP2 stronger to improve robustness of the circuit. At this time M2 & M3 are ON and helps to hold a high voltage at the gate of keeper transistor MP2. After a delay of 2 x $\tau_{inv,}$ M3 turns ON whilM2 remains ON. As aresult MP2 turns OFF completely while MN1 turns ON to speed-up the evaluation process.

After 4 x $\tau_{inv,\ M2\ turns\ ON,}$ resulting in OFF path from V_{DD} to node. At this time, M4 keeps MP2 OFF for the rest of the evaluation phase. Assuming all inputs at "0", M4 connects the gate of MP2 to ground which turn on the keeper transistor MP2 and helps to hold the dynamic node.

The speed of the circuit is determined by the transistor which plays a critical role. At mode E voltage level is lowered to V_{DD} - V_{th} due to using NMOS transistor M1 connected to the gate of keeper transistor. Hence current through keeper transistor increases which results in improving robustness but performance degraded.

4.5 LCR keeper dynamic gate topology

As shown in fig. 11. The short comings of the conventional keeper addressed by the leakage current replic(LCR) which uses conventional analog current mirror. It tracks any process corner as well as voltage and current. A single current mirror structure can be shared among more than one one dynamic gates.

LCR keeper = 1 FET /dynamic gtes + portion of shared current mirror crcuit.

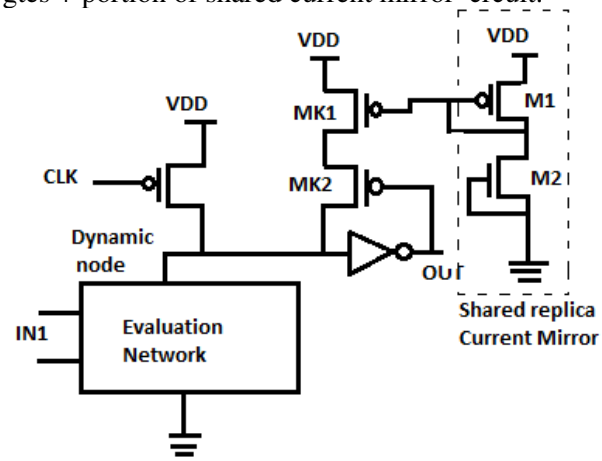

Fig.11. Leakage current replica (LCR)

4.6 Implementation of wide OR gate using CCD concept

As shown in fig. 12. Current-comparison domino concept utilizes pull-up-network (PUN) rather than pull-down-networkm (PDN) because there is a race between I_{PUN} and I_{Ref} current. When output node voltage fall to ground voltage, M_k is added in series with the reference current in order to reduce power consumption.

In order to maintain robustness of the designed circuit, generation of the reference voltage is of great issue. As we know that there are process variations due to random and systematic fluctuations. So, reference current must vary with the variation of the process to maintain reference voltage. Here threshold voltage of all nMOS transistors varies together and all pMOS transistor varies together. Speed of gate, power consumption and noise immunity is directly affected by the any threshold voltage variations of node A & B as in fig. 13.

The major drawbacks is that the threshold voltage of nMOS is decreased and that of pMOS is increased. This circuit is similar to replica leakage circuit proposed by [12]. A series diode- connection transistor M6 similar to M1is added. The gate of transistor M7 is connected to VDD to track leakage current variations due to process variations. The circuit shown in fig. 13 proposed by [2] explained in two phases as follows.

A. Precharge Phase

CLK= "0", $\overline{CLK}$ = "1", Input signals are high and clock voltage is low levels. The voltages of the dynamic node (Dyn) and node A have fallen to the low levels by transistor M_{Dis} and raised to the high level by transistor M_{pre} respectively. Transistors $M_{pre,}$ $M_{Dis,}$ M_{k1} and M_{k2} are ON and transistors M_1, M_2 and M_{Eval} are OFF. The output voltage raised to high level by the output inverter.

B.Evaluation Phase

Here, CLK= "1", $\overline{CLK}$ = "0", and input voltage in low level. Transistors M_{pre} M_{Dis} are OFF and transistors M1, M2, Mk2 and MEval are ON and transistors Mk1 can become On or OFF depending on input voltages. First all input

signals are high and a small amount of voltage is established across transistor M1 due to leakage current. This leakage current is mirrored by transistor M2, the keeper transistors of the second stage (Mk1 and Mk2) compensate this mirrored leakage current. Speed increases due to upsizing the transistor M_1 and increase in mirror ratio (M).

$$M = \frac{\left(\frac{W}{L}\right)M2}{\left(\frac{W}{L}\right)M1} \quad (4)$$

In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage which is equal to gate-source voltage of the saturated transistor M_1. Also, this voltage is equal to drain-source voltage of transistor M2. Thus increasing the pull-up current , the mirrored current of M2. Hence dynamic node Dyn is charged to V_{DD} which discharge the output voltage amd turning OFF the main keeper transistor M_{k1}. So, contentation current between the keeper transistor and mirror transistor is reduced.

This designed circuit is simulated using HSPICE in high performance 16-nm predictive technology [13] at temperature 110^0 C. 8,16,32,64 input wide fan-in OR gate is used as a benchmark operated in 1-GHz frequency. 0.8v is used as supply voltage in simulations and output capacitance is set at 5F.

Here, noise margin matrix is known as unity noise gain (UNG) proposed by [14].
Matrix is shown by

$$\mathbf{UNG}= \{V_{in} : V_{noise} = V_{output}\} \quad (5)$$

Amplitude of the input noise is equal to output . In this method, a pulse noise produces cross talk type of noise which increases with increasing noise pulse duration.

A figure of merit (FOM) to account for noise, delay, power and area together for the design of a logic gate such as OR gate is defined as

$$\mathbf{FOM}= \frac{UNG_{norm}}{P_{tot-norm} \times t_{p-norm}^2 \times \sigma_{Delay-norm} \times A_{norm}} \quad (4)$$

Where UNG_{norm}, $t_{p\text{-}norm}$, $\sigma_{Delay\text{-}norm}$ and A_{norm} are the UNG, worst case propagation delay, standard deviation of delay and total area of circuit respectively. All these are normalised to the value for 64-input SFLD OR gate. Since wide fan-in (8,16,32,64 input) OR gate are implemented by using these circuits in the same delay i.e. 50, 50, 60 and 70 psdelay for 8, 16, 32, 64-input in OR gate respectively. Desired delay is achieved by sizing of the transistors. For all circuits, the width of the transistors in the OR gate block is set to the minimum width which is equal to $W_{min} = 7L_{imn}$. Where Lmin = 16nm. The width ratio of pMOS to nMOS transistor of the inverters is set to 2.

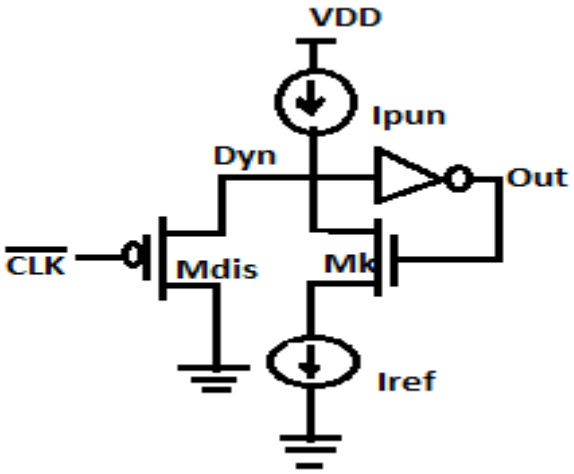

Fig. 12. Concept of Current-Comparison (CCD)

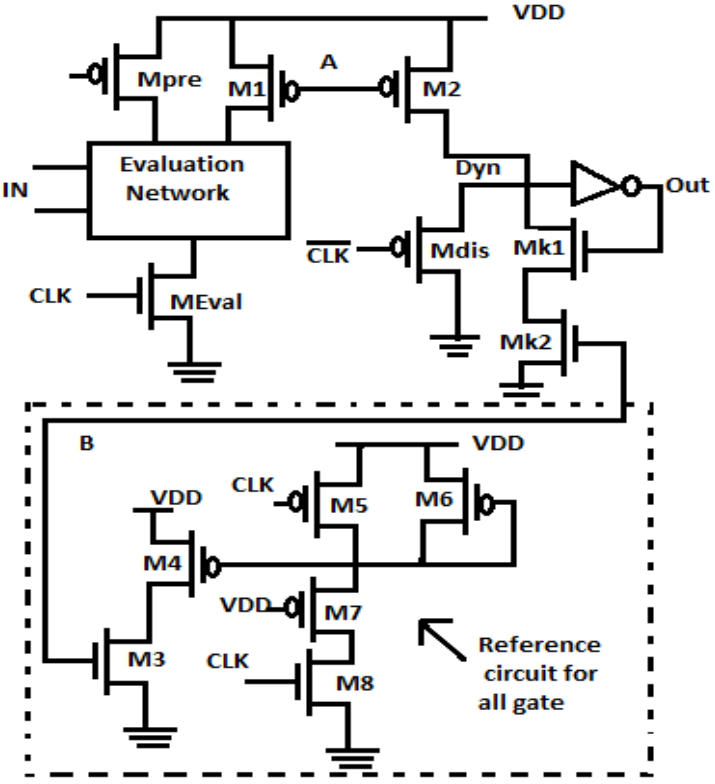

Fig.13. Implementation of wide OR gate using CCD

5. Domino logic circuit using FinFET

In order to achieve better controllability of the channel, introducing significantly lower sub-threshold and gate leakage current as compared to the conventional CMOS devices, one move to the FinFET based circuits. FinFET device is having two gates. Hence better control. Moreover, decreased Drain Induced Barrier Lowering (DIBL) due to reduced effect on the channel from drain to source. Also, reduced random dopant fluctuations is achieved by fully-depleted channel.

Implementation of Footed domino logic (FDL) using FinFET(Lg=32nm) is shown in Fig. 14. In this design replacement of CMOS device with FinFET in the existing FDL circuit is done. FinFET domino logic gives better performance in a lower leakage power due to reduced short channel effect and a better controllability of the channel. Power comparison under iso-delay for different circuits are shown in fig. 15. Hence, robustness of the FinFET implementation improves significantly due to reduced leakage current through NMOS network.

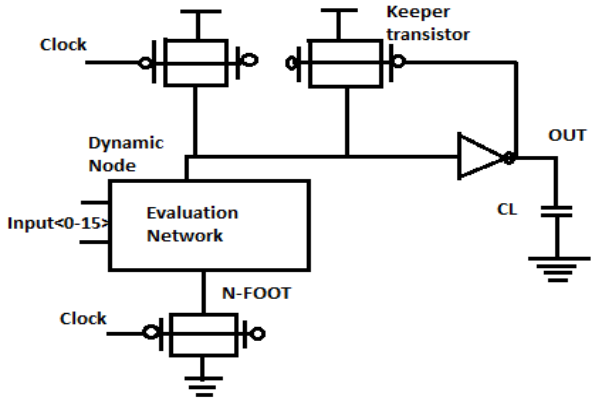

Fig. 14. FinFET Footed Domino Logic

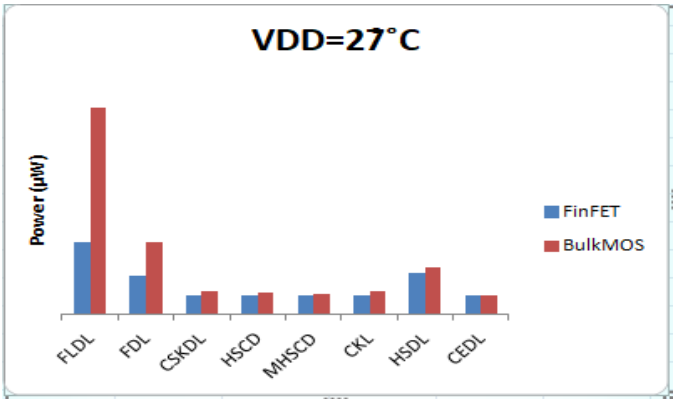

Fig.15. Power comparison for FinFET and Bulk MOS

6. SIMULATIONS & RESULTS

TABLE I

Power comparison for different domino logic Techniques for 16-OR gate

Domino Logic Circuits	Power (μW)
SFLD	12.9
FLDL	88.9
FDL	32.6
HSDL	22.5
CKL	10.3
CMFDL	10.7
HSCD	8.24
MHSCD	8.37
CEDL	8.08
CSKDL	22.5
LCR	13
CCD	8.6

TABLE II

Comparison of Normalised UNGs (Under Same Delay)

Fan-in		Standard Footless domino (SFLD)	High Speed domino (HSD)	Leakage current replica (LCR)	CKL	CSKDL	FDL	CMFDL	Current domino (CCD)
8	UNG	0.41	0.42	0.21	-	-	-	-	0.8
	Normalised UNG	1	0.9	0.51	-	-	-	-	1.95
16	UNG	0.33	0.31	0.27	0.18	0.45	.17	0.6	0.8
	Normalised UNG	1	0.94	0.82	-	-	-	-	2.42
32	UNG	0.28	0.26	0.32	-	-	-	-	0.8
	Normalised UNG	1	0.93	1.14	-	-	-	-	2.86
64	UNG	0.22	0.2	0.4	-	-	-	-	0.53
	Normalised UNG	1	0.91	1.82	-	-	-	-	2.41

Table I shows comparative analysis of power consumption in different techniques. It shows approximately 10X power consumption as compared to FLDL. **Table II** shows simulation result of unity noise gain (UNG) for different domino circuits at same delay. The result obtained , indicate from 2.42 to 3.20 times improvement over FDL.

7. CONCLUSION:

In this analysis paper, several domino logic circuits design are analysed. Analysis of the domino logic circuits such as CMFDL, HSCD, MHSCD, CEDL and CSKDL showed at least 3.5X improvement in UNG compared to the conventional design. Leakage current of the evaluation network of dynamic gates was increased with technology scaling in wide domino gates which reduces noise immunity and increased power consumption. Moreover, increasing fan-in not only reduces worst case delay but also increases the contention between the keeper transistor and the evaluation network. Hence, a new circuit design called CCD was proposed in [2]. Increased robustness with low leakage without significant performance degradation or increased power consumption was the main goal of the CCD design. Several existing circuit designs were simulated and compared. Simulation results demonstrated significant progress in leakage reduction and acceptable speed for high speed applications. As compared to other design CCD has very high UNG for wide fan-in OR gates. Moreover, after analysing the CCD design, we come to conclusion that it is suitable for implementing wide fan-in Boolean logic functions with high noise immunity, lower area consumption, time delay and power consumption.

Furthermore, when all the bulk CMOS devices are replaced by FinFET devices, we come to the conclusion that robustness of the FinFET implementation improves significantly. Simulation is done using TCAD tools, Taurus. FinFET designs give significantly lower leakage compared to utilizing bulk CMOS device. Simulation results show 2.7 times less power consumption of conventional domino circuit by using FinFET comparing with Bulk CMOS devices.

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