DESIGNING OF D FLIP-FLOP USING DUAL EDGE TRIGGER

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Abstract: *In the current study the using double edge triggered (DET), instead of, conventional single edge triggered (SET) flip-flops. We begin the paper by introducing a set of novel D-type double edge triggered flip-flops which can be implemented with fewer transistors than any previous design. They examine includes a development self study on the response of I/p arrangement in the power distraction of single and double edge triggered flip-flops. The system balanced power savings achievable by utilizing registers exist of double edge triggered flip-flops, rather of single edge triggered flip-flops, is afterward analyze. The results are greatly bright, signify that double edge triggered flip-flops are able of symbolic power savings, for a small reduce in complication.*

Key Words: *D flip flop, edge triggered, SET.*

1. INTRODUCTION:

In the previous, the bigger involvement of the VLSI designer were area, performance, amount and accuracy, in current years, this has start to advance and, progressively, energy is being given comparison weight to area and speed in VLSI design. One of the primary driving factors has been the remarkable success and growth of the class of wireless communications systems (personal digital assistants and personal communicators) which demand high-speed and complex functionality with low power consumption. Many digital circuits are used synchronous circuits for designing because it reduces the complexity of circuit design. Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. The clock intervals to collect and manage data for a short time period enough for different circuits within a system to another operation data. Energy dissipation is an valuable guideline in the design of VLSI circuits, and the clock structure is answerable for a important part of it (up to 50%). When the supply voltage is decreased the speed of the logic circuits might be diminished due to reduction in effective input voltage to the transistors. Mostly without accurate power prognostication and enhance tools the design for low power issues can't be overcome. So calculate the power dissipation in digital circuit it necessary to use certain tools during the design to meet the power constraints to avoid the costly redesign effort. Edge triggered flip-flops are most used synchronous digital circuits. D-type flip-flop is the fundamental building blocks in current VLSI systems and it display contribution of the total energy dissipation in digital system [12]. In synchronous VLSI circuits all clock energy utilization is done in the clock circuits, clock buffers, and the flip-flops [3]. There are many factors where the Power consumption is dependent, as $P = \alpha C f$ [5] here the power is proportional to the square of the voltage. To reduce power consumption the voltage scaling is the most effective way. Also voltage scaling is associated with threshold voltage scaling which can be creating leakage power to increase exponentially. Using double-edge triggered flip-flops, the clock frequency can reduced ideally, while the rate of data processing. Paper is charge the clarifies the agreeing DETFF circuit. Correlate latest proposed design and conforming designs in conditions of normal energy, delay. Paper ends with the deduction. Double Edge Triggered Flip Flop's can be implemented in various ways for reduced of power consumption and minimum delay by using transmission gates such designs are having clock signal internal and external as well. In the flip-flop is fundamentally a Master Slave flip-flop arrangement. With two data paths. The upper data path reside of a Single Edge Triggered flip-flop integrate using transportation gates. This works in positive edge. The lower data path reside of a negative edge triggered flip-flop integrate utilizing transportation gates. Both the data paths have feedback loops connected such that, whenever the clock is stopped, the logic level at the output is retained.

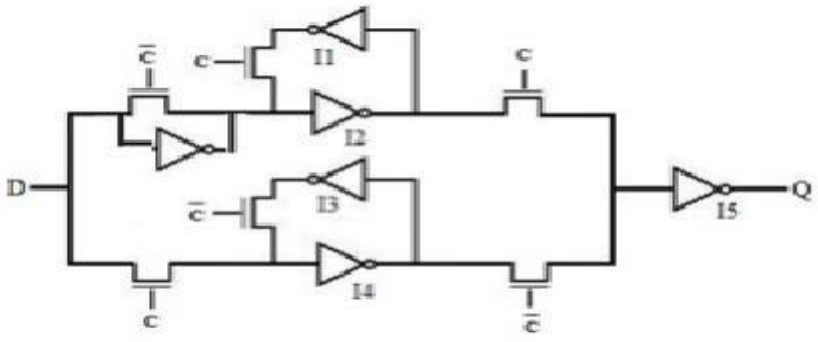

Fig.1 FET

DET flip-flop is except that feedback has been changed. On rising edge the upper data path is triggered and on falling edge lower data path is triggered an inverter and a PMOS transistor are used to hold the logic level when the Transmission gate is closed. When the data value high, the inverter is switch the signal to low, so will be make the PMOS transistor which pull the data up to the high. When value of data is low then the inverter switch the signal to high, which will isolate the data from VDD and keep the value low. For high output, this type of flip-flop is give static functionality since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. It will create the circuit to react like a dynamic circuit. As shown in Fig 2.

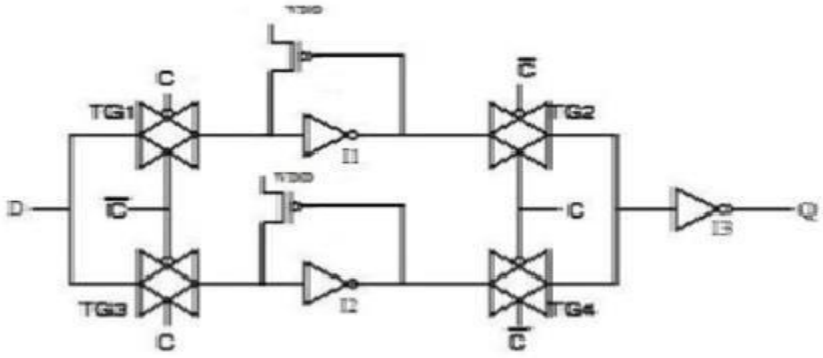

Fig. 2 DET

2. PROPOSED TECHNIQUE

The Double Edge Triggered Flip-Flop layout is define. The allowable unit of flip-flop is a Master Slave flip flop that exists of two data paths. The proposed flip-flop's operation is same to that, but number of clocked transistors is reduced from 10 to 6 by replacing the transmission gates by using n-type pass transistors. Shown in figure is built by utilizing sub-circuit design. Also W/L ratio is adjusted for making the transistors working in saturation region. Basically, n-type pass transistors give weak high but the n-type pass transistors is followed by an inverter, which results in strongly high. The expected DETFF is free threshold voltage loss difficulty of pass transistors. The feedback structure is replacing the p-type pass transistor and n-type pass transistor the area NMOS is less PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors. Thus the proposed Design has become more efficient in terms of area, power and speed which showing better performance compare to conformist designs. As shown in Fig 3.

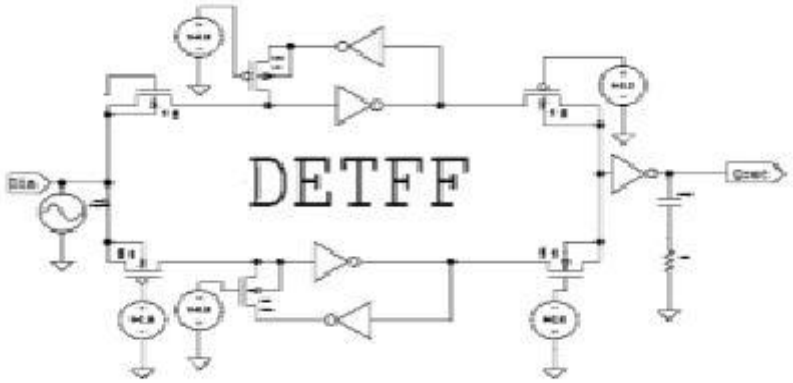

Fig.3 DETFF

3. PROPOSED WORK

The proposed double edge trigger flip flop utilizes the relative complexity of the equal logic and greater/smaller. Following subsection first introduces the proposed double edge trigger flip flop architecture followed by complexity analysis.

In this section, the area reduction gain of the afros mentioned methodology is evaluated by applying it to a video decoder design. In the reader can find a variety of RVC-CAL applications for dataflow programs. One of these applications is the intra MPEG-4 simple profile decoder. Due to restrictions on the number of clock buffers in Xilinx FPGAs, the design selected was re factored to result in 32 actors.

A. Test Design The intra MPEG-4 SP description contains 32 actors and it is 4:2:0 decoder which is separated into eight processing blocks. As shown in Fig 4.

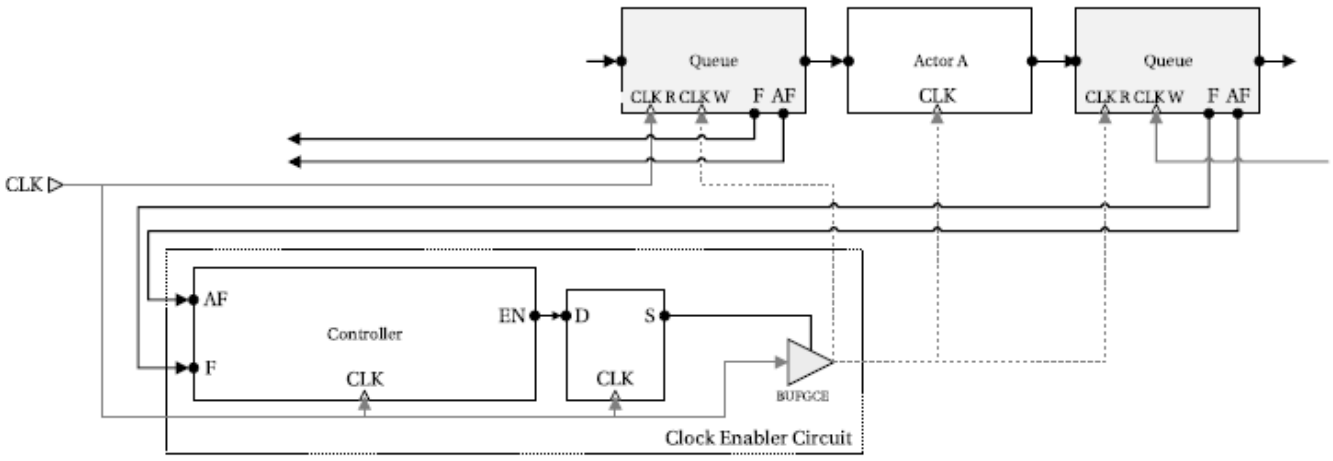

Fig. 4 streaming application element (De-blocking filter) with clock gating.

There are five main components in this architecture. The first component is the two block memories to store the data received from an external memory. Each memory is a 32 bit dual-port SRAM. Block Memory 1 is used to store the left neighbour blocks (E1-E8) for Filter Unit 1. Block Memory 2 is used to store the top neighbour blocks (F1-F8) for Filter Unit 3. The second component is Filter Units including two horizontal filters and two vertical filters. Filter Unit 1 and Filter Unit 2 are two horizontal filter modules, HF1 and HF2. Filter Unit 3 and Filter Unit 4 are two vertical filter modules, VF3 and VF4. In addition, a RAM Transposer, which is used to transpose the data flow of 8x8 blocks from row to column in order to help reuse the data of the horizontal filter for the vertical filter without storing back to the memory. As shown in Fig 5.

Parallel De-blocking Filter as an Actor unit

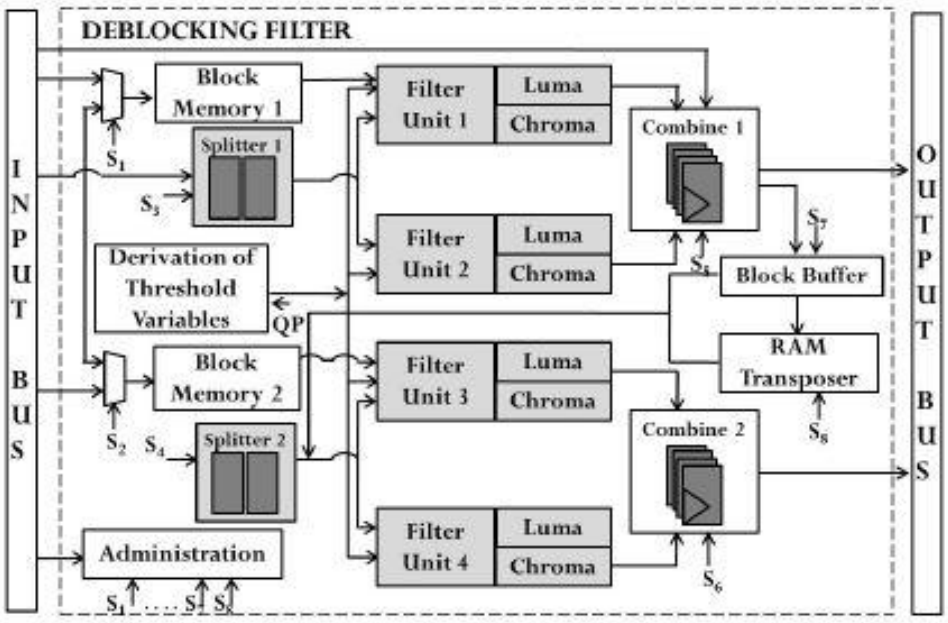

Fig. 5 The block diagram of the proposed parallel de-blocking filter architecture.

4. SIMULATION RESULTS

After apply such innovative in DETFF we got the better result in terms of performance and number LUTs. The area is reduced to reach the new level. As mentioned the LUTs have been reduced it means that the occupied area is less than the exiting SETFF.

Table 1- Single edge trigger flip-flop

Logic utilization	used	available	utilization
Number of slices	3517	4656	75%
Number of slice flip flops	4288	9312	46%
Number of 4 input luts	2760	9312	29%
Number of bonded IOBs	55	232	23%
Number of MULT 18X18SIOs	8	20	40%
Number of GCLKs	1	24	4%

Table 2- Double edge trigger flip-flop

Logic utilization	used	available	utilization
Number of slices	105	4656	2%
Number of slice flip flops	176	9312	1%
Number of 4 input luts	74	9312	0%
Number of bonded IOBs	45	232	19%
Number of MULT 18X18SIOs	8	20	40%
Number of GCLKs	1	24	4%

We observe from table 2 that LUTs used by design is 74 whereas the total available LUTs are 9312 which around zero percent so we can conclude that the developed system is very much reliable as well as efficient in term of area. The factor we have observed in the list is number of bonded IOBs in this section we used 45 IOBs whereas total available IOBs are 232. We have use 19% of IOBs of device. The number of LUTs is reduced as compare to SETFF. In short we can say that the developed device is efficient in term of area.

To check the functionality, created test bench. The applied pattern at the input provides correct output and the simulation waveform is show in Figure 6.

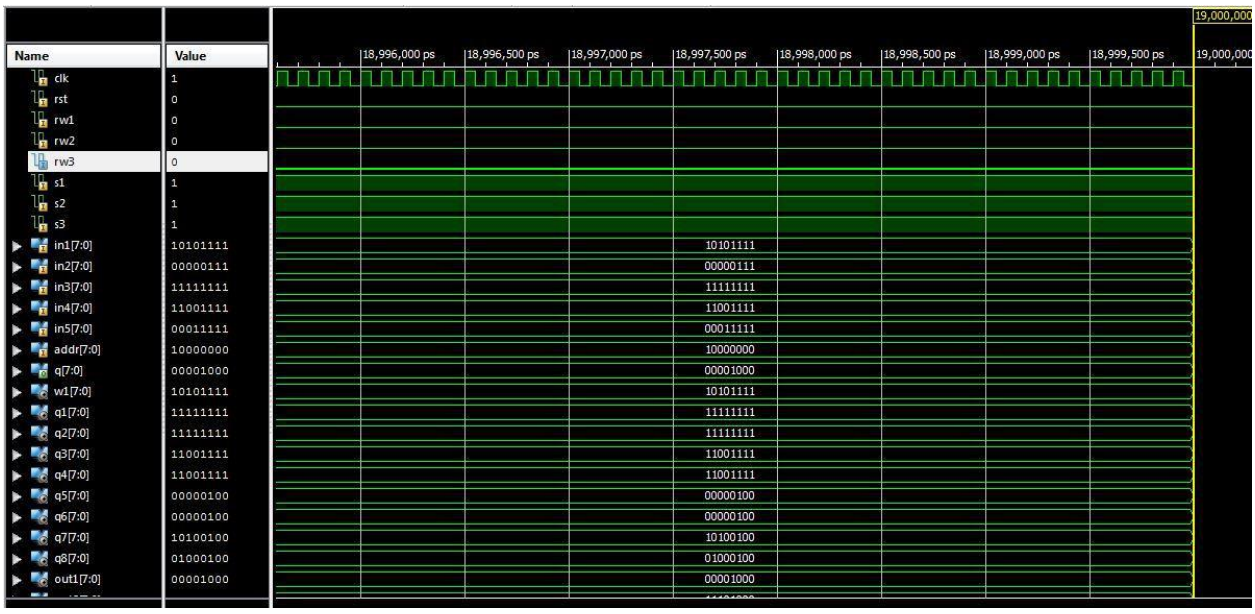

Fig. 6 waveform showing inputs and output.

5. CONCLUSION:

In this paper explored that the existing SETFF architectures and presented a new DETFF that shows significant improved performance over the existing SETFF architecture. The proposed and existing flip flop are

implemented in Xilinx tool. The designs are synthesized and post synthesis results are extracted. The simulation results are reducing the area over existing architecture. Thus the proposed flip flop can be effectively utilized.

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