DESIGN AND IMPLEMENTATION OF OPTIMIZED ALU

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Abstract*: VLSI (Very large scale integration) consisting of millions of transistors on a single chip is the technology for the revolution in computers, communication and electronics. Demands for the low power VLSI have been pushing the development of modern design methodologies to reduce the power consumption and to increase speed drastically. In order to meet the growing demand of low power VLSI systems, a low power ALU circuit is proposed by using clock gating techniques type of design which considerably increases the speed and decreases the power consumption.*

An (ALU) is a major subsystem in a computer. It can perform all types of arithmetic and logical operations. By using scaling, it can provide high performance, more functionality and less power dissipation. Now a days these measures became major bottleneck for system design. In ALU, one functional unit is working other functional units remain idle but they are connected to clock and all units dissipating significant amount of power. By using clock gating techniques, a significant amount of power saving can be achieved.

Key Words: *Architecture, Low power, Clock Gating, ALU, Simulation.*

1. INTRODUCTION:

Low-power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products. Present day general purpose Processor designs are faced with the daunting task of reducing power dissipation. Since power dissipation is becoming a bottleneck for future technologies, lowering power consumption is important for not only lengthening battery life in portable systems, but also improving reliability and reducing heat removal cost in high performance systems. The ALU is one of the important functional blocks of a System.

Arithmetic and Logic Unit (ALU) is one of the common and the most crucial components of any system. Power consumption is a major design issue in the case of VLSI & Embedded systems. Usually ALU's consists of a number of functional units for different arithmetic and logic operations which are realized using combinational circuits. Each of the functional unit performs a specific arithmetic or logic operation. In this paper the main concern is given for reducing the power of the adder and multiplier modules which are important functional units of ALU thereby reducing the overall power consumption without compromising the speed of the processor. The ALU circuit ensures the execution of either arithmetic or logic operation only at a time so that only one set of circuits is active at a time thus ensuring low power consumption.

In the earlier days, the designers of VLSI were more interested on the area of the circuits, performance, reliability and cost was also the main consideration and power consumption was their minor consideration. Now-a-days, the power is also being given equal importance in comparison to area and speed. In today's world the demand is more functional, energy efficient and optimized power devices. With modern day computers becoming faster and faster and by extension consuming more and more power there is a drive to design new computers with lower power consumption. With advancement in technology, the number of transistor count on a single CPU has increased. Integrating these transistors for power enhancement will also have an impact on power consumption because adding more and more transistor will give rise in the heat dissipated in the device.

Since most of the portable devices are battery driven the power consumption of these devices must be low so the battery life improves, reliability improves etc. Because of these reasons power management has become an important design constraints for most the computationally intensive and sophisticated applications. ALU is one of the most important units in a microprocessor and it performs most of the computational operation in a CPU and hence power consumption is an important issue in an ALU. To develop low power processor, low power ALU is developed since ALU is a basic integral part of any processor. Clock power is a major component of microprocessor power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. Thus the total clock power is a substantial component of total microprocessor power dissipation. Most of the power dissipation is of the dynamic type which necessities the reduction in switching power dissipation. Fig 1 shows the power distribution

among different units of a recent high-performance CPU. The clock is the largest power consuming component which includes clock generator, clock drivers, clock distribution tree, latches, and clock loading due to all the clocked elements. Out of these, clock loading shares bulk amount of power. The main effect of power dissipation is the heat dissipated by the device. The increase in temperature results in decrease in life time of the transistors. This affects the reliability of the device.

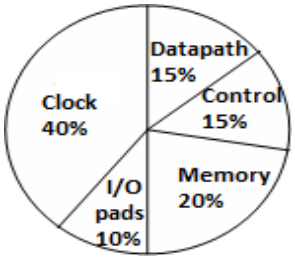
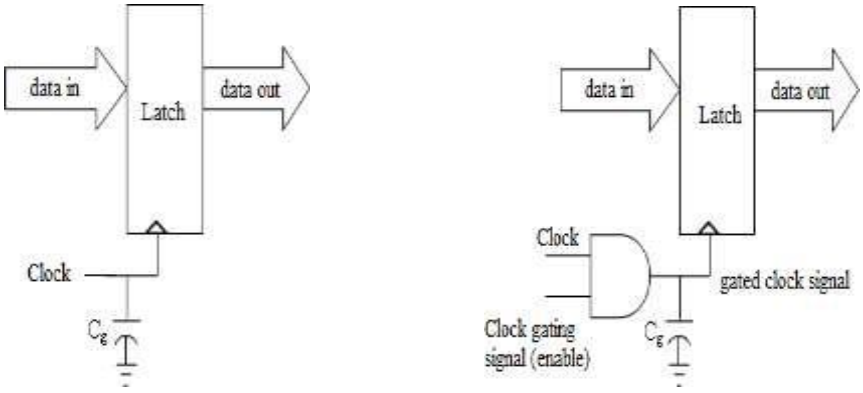


Figure 1: Processor Power Distribution

2. CLOCK GATING:

Several techniques to reduce the power consumption have been developed, of which clock gating is predominant. It is the most popular method for power reduction of clock signals and functional units. Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems The clock gating techniques have been developed to avoid unnecessary power consumptions, The basic principle behind this power optimization technique is if the clock signal is gated with the enable signal, if both the signals are active then only the output will come otherwise not .So whenever the output of the particular operation is not needed, unwanted switching activities will be suppressed and hence the power reduces. So Clock-gating is a technique where the clock signal is prevented from reaching the various modules of the ALU. Here enable signal acts as the control signal which is shown in figure. But Clock gating does not come for free.

Clock gating is achieved by ANDing the clock signal with a control signal to form a gated clock, which is then applied to different components of the circuit. To which module the gated clock should be applied is decided based on the control signal. Hence based on the enable signal and clock, if both the signals active then only particular operation will be done and the other operations remain idle. The enable signal is controlled by the selection control in the present design. This is shown that the clock-gating technique help in reducing the power consumption of the ALU, this technique i.e clock gating help in reducing the power greatly at high frequencies.



(a) **(b)**

Figure 2: Schematic of latch element (a) without and (b) with clock gating

3. PROPOSED ARCHITECTURE:

The data path elements are the functional blocks within a Processor that actually interact to perform computational operations. These tasks include reading from/writing to memory and register file, and arithmetic and logical operations.

In the proposed work, 16 bit ALU of the shown in figure 5, which performs eight arithmetic and eight logical operations selected by 4 bit code, figure 3 shows inputs and outputs of ALU. Instead of designing ALU as a single module, it is divided into four functional blocks, namely, ARTH_1, ARTH_2, LOGICAL_1 and LOGICAL_2.

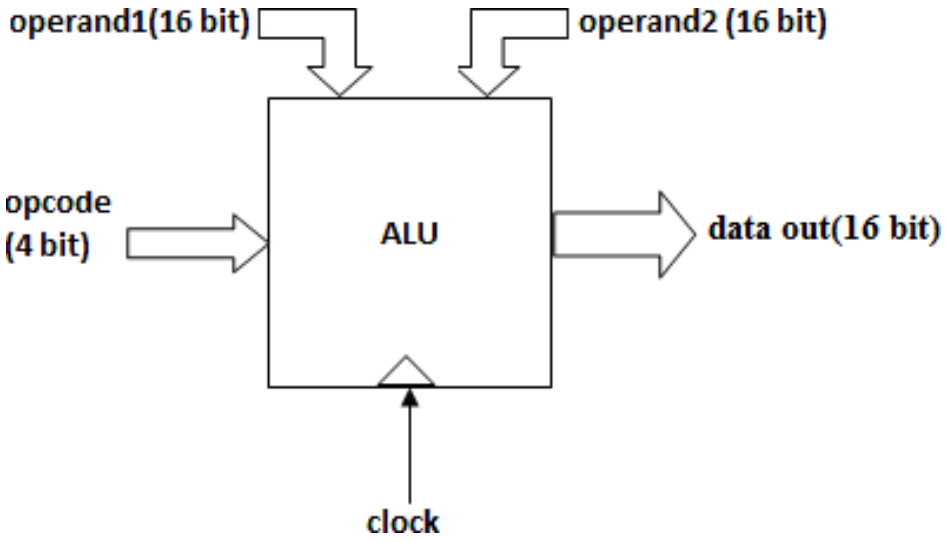


Figure 3: Proposed ALU module

Each block performs four different operations as shown in the functional Table 1. ALU takes 16 bit operands as inputs, process the Operand data and gives 16 bit output data.

Figure 4 shows clock distribution in proposed ALU in which clock signals are not directly connected to the functional units (FUs) of ALU section. Instead, clock signals are gated with coded signals and are fed to the desired functional units. For example, while ARTH_1 is performing operations, remaining functional blocks ARTH_2, LOGICAL_1 and LOGICAL_2 are not performing any operations, such that, clock signal is delivered only to ARTH_1 functional unit.

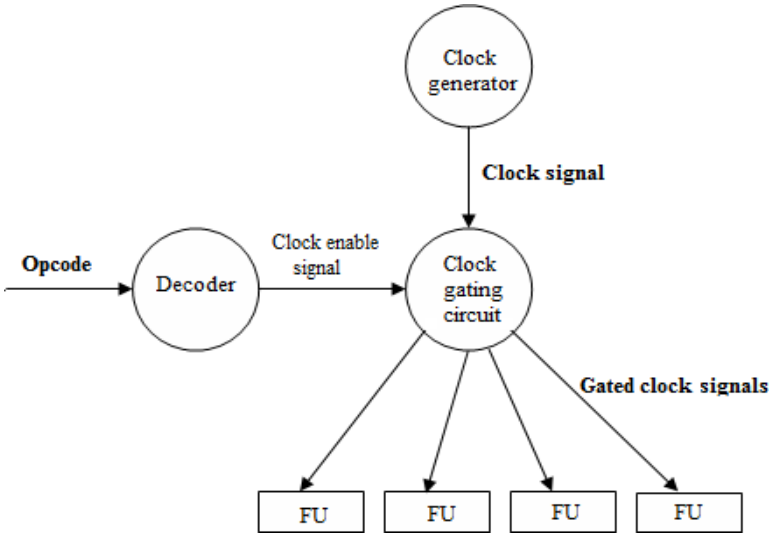


Figure 4: Clock distributions in proposed ALU

The internal architecture of ALU is shown in figure 5, which consists of a 2 to 4 decoder, clock gating circuit (array of AND gates), four functional units and one multiplexer. Decoder unit decode the opcode and generates clock enable signals, clock gating circuit generates gated clock signals to desired functional units, functional units perform operations as given in Table 1, and multiplexer selects one of the functional unit outputs. Two out of four select lines are used to select the required operation. The proposed ALU operation can be explained as follows: D3D2 bits of the opcode selects one of the functional units and M1M0 bits selects required operation. For example, when opcode is "0100", 01 bits selects clock signal to the ARTH_2 unit, while for remaining units clock signals are not allowed. Bits 00 enables ARTH_2 unit to perform multiplication operation, the same bits/ lines used to select appropriate output from outputs of functional blocks with the help of MUX. Typically, the core of the ALU consists of functional units which take operands from register file, data cache or ALU write back bus. The ALU output is multiplexed with the logical output through an output multiplexer.

4. Functions of ALU:

Opcode ($D_1D_0M_1M_0$)	Operation	Active block
0000	Addition	ARTH_1
0001	Subtraction	
0010	Increment	
0011	Decrement	
0100	Multiplication	ARTH_2
0101	Division	
0110	Modulus	
0111	Power of n	
1000	AND	LOGICAL_1
1001	OR	
1010	NOT	
1011	EXOR	
1100	NAND	LOGICAL_2
1101	NOR	
1110	Shift left	
1111	Shift right	

5. Internal architecture of proposed ALU:

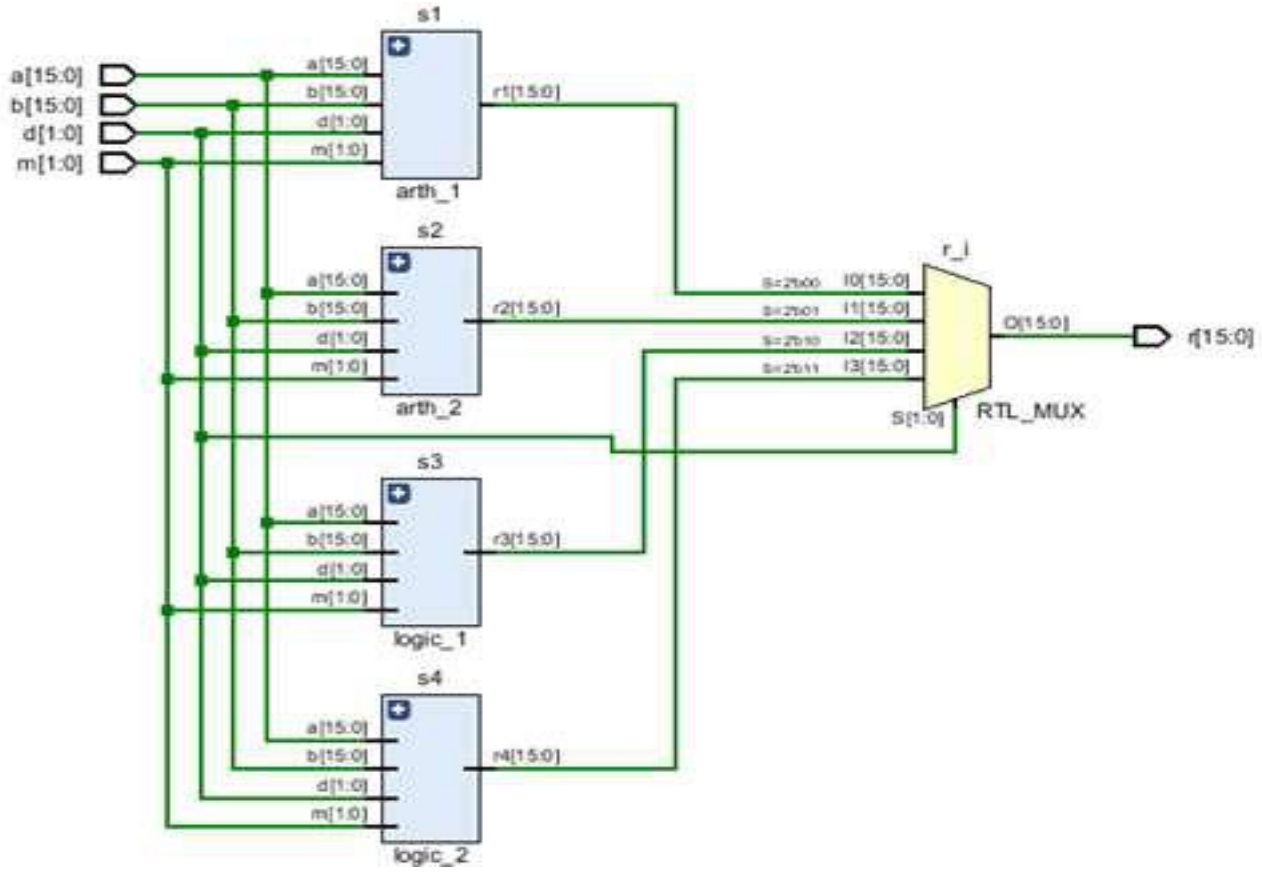


Figure 5: Internal architecture of proposed ALU

While ARTH_2 is performing operations remaining functional blocks ARTH_1, LOGICAL_1 and LOGICAL_2 are idle. As shown in figure 5, gated clock signals generated by the decoder controls the charge/discharge of the capacitance, Cg of the unused blocks thus saving clock power.

6. IMPLEMENTATION:

Flow chart for clock gating circuit is shown in figure 6. Only when the clock event and clock enable signal occurs it allows clock signal to the required module.

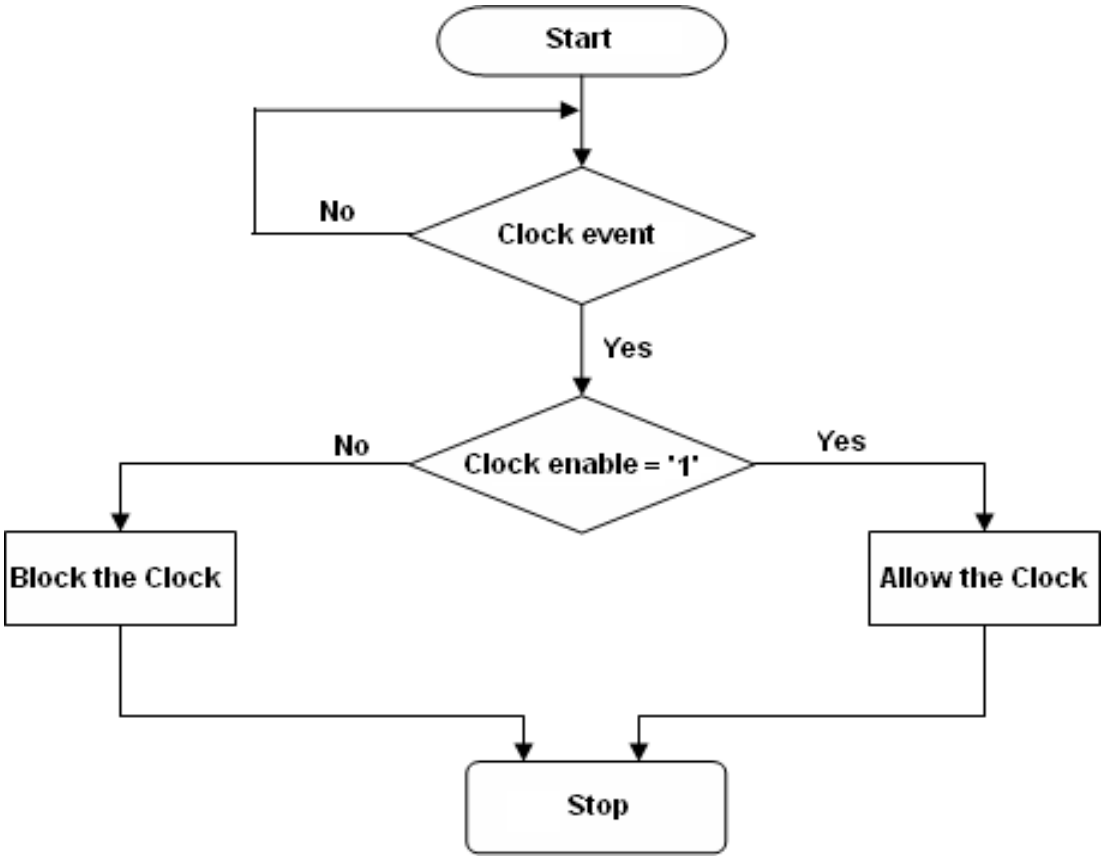


Figure 6: Flow chart for Clock gating circuit

The whole design is captured using VHDL language. The architecture of proposed ALU shown in figure 5 is implemented in different modules to get the desired functionality. The following steps are followed during implementation of this design: Code generation, Simulation, Synthesis, Power analysis, RTL schematic and Technology schematic.

7. RESULTS:

Simulation and Synthesis:

The simulation results of ALU unit are presented in figure 7. The input signals are **Alu Oprand 1(16 bit), Alu Oprand 2(16 bit)** and the output signals are **Alu out (16 bit)**. For example, when the opcode is "0100", it performs multiplication operation.

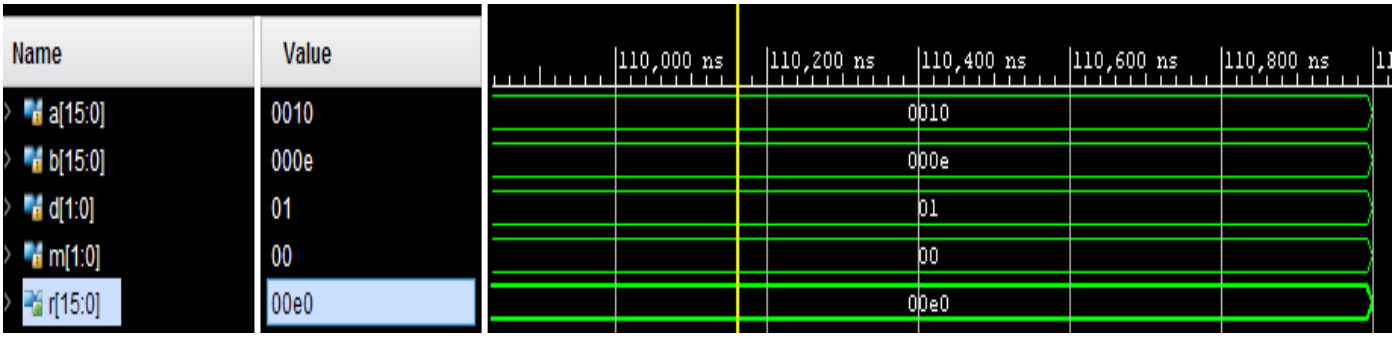


Figure 7: Simulation results of ALU

The RTL viewer of ALU is shown in figure 8. From this figure, it can be observed that the clock gating circuit controls the clock for different sections of ALU.

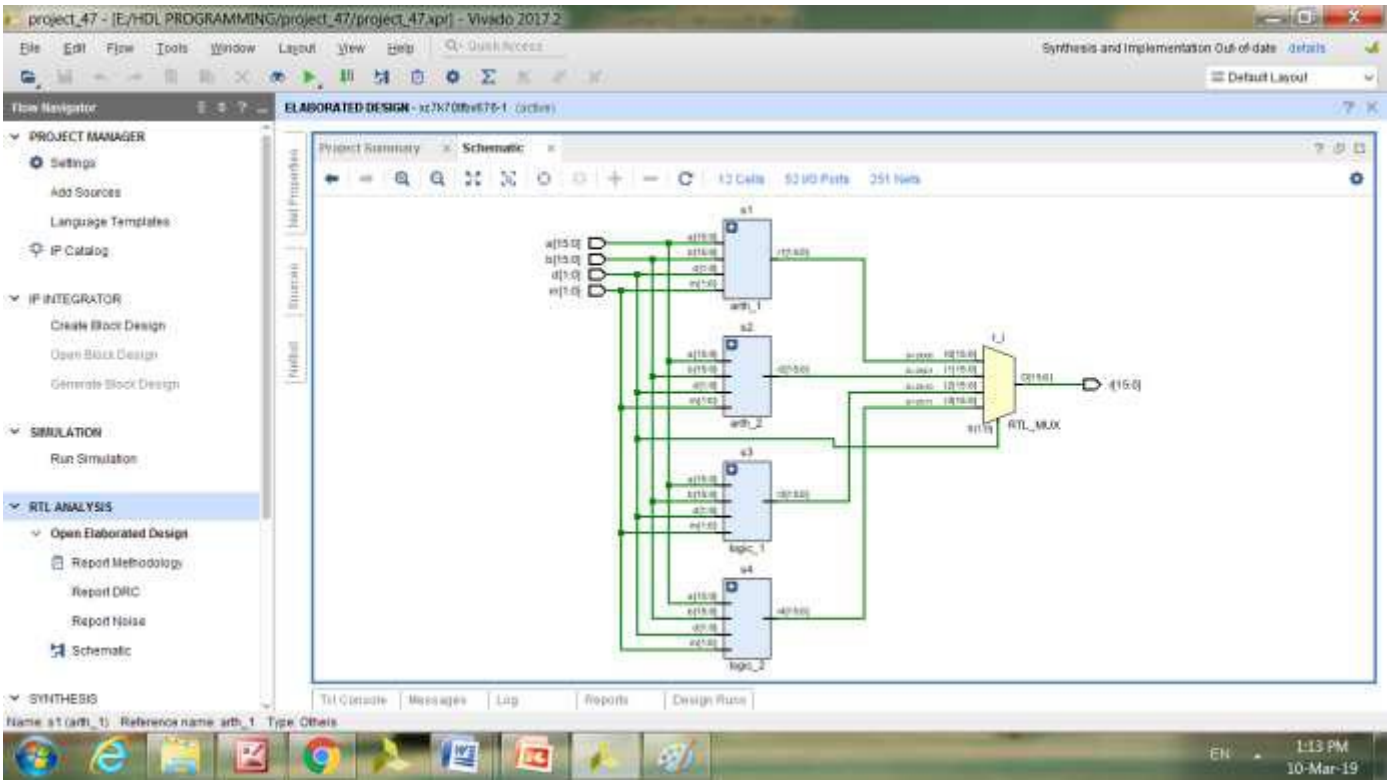


Figure 8: ALU RTL Schematic

The Implemented Schematic of ALU is shown in figure 9. This view shows a technology-level representation of ALU in terms of logic elements such as LUTs, carry logic, I/O buffers, and other technology-specific components - all HDL optimized to the target Xilinx device.

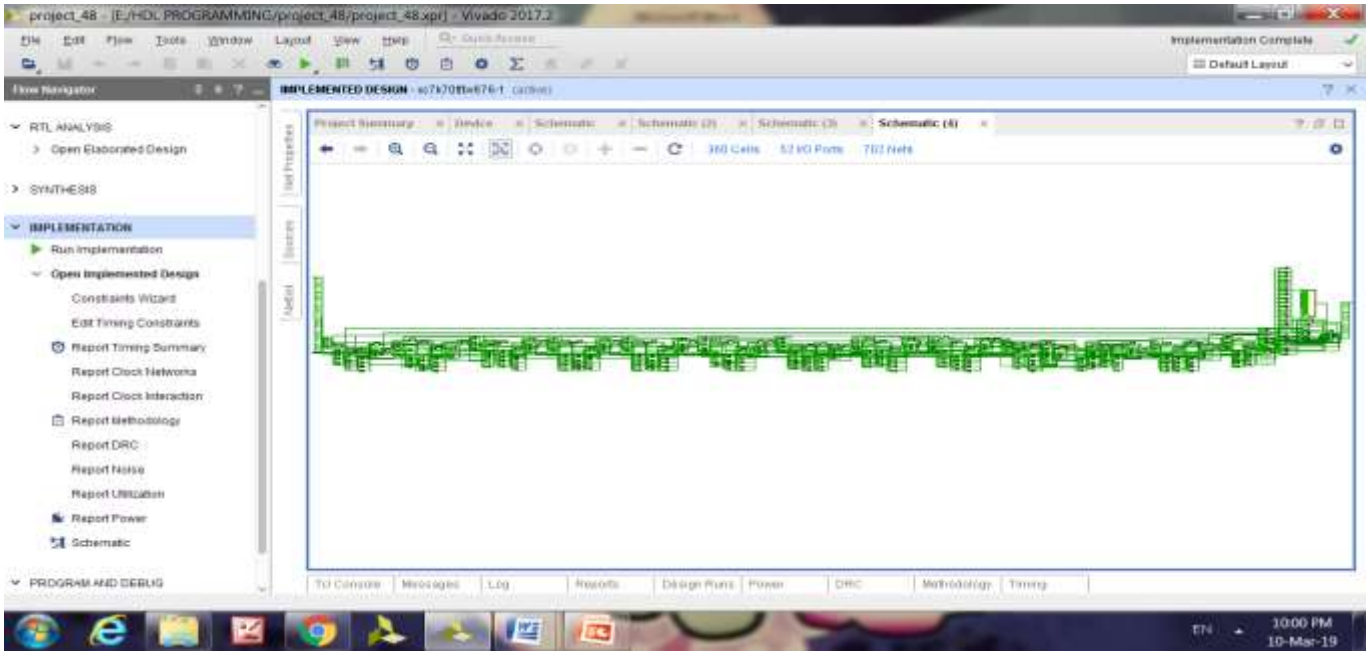


Figure 9: ALU Implemented Schematic

The Implemented Design of ALU is shown in figure 10. This view shows a technology-level representation of ALU in terms of logic elements such as LUTs, carry logic, I/O buffers, and other technology-specific components - all HDL optimized to the target Xilinx device.

Figure 10: ALU Implemented Schematic

Power Analysis:

Power analysis of low power ALU is carried out by using Xilinx's VIVADO analysis tool. Figure shows variation of power dissipation with operating frequency for various supply voltages. It is observed that ALU is dissipating a power of 23.285mW at a frequency of 15MHz under no load conditions.

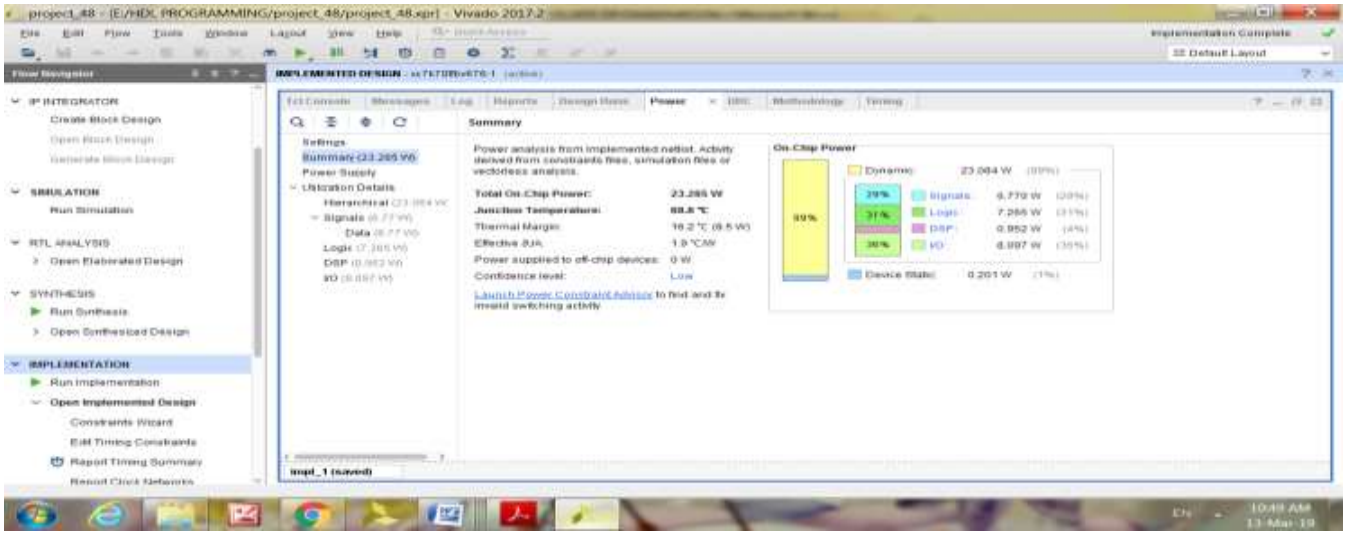


Figure 10: Variation of power dissipation with operating frequency for various supply voltages

Characteristics of ALU chip

Precision	16 bit
Architecture	low-power
Maximum Frequency (MHz)	281.770
Power Dissipation (W)	23.285 *@15MHz*
Supply Voltage (V)	2.4

No. of functions	16
No. of pins	53

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8. CONCLUSIONS:

Power dissipation is becoming a limiting factor for high performance Processor design due to ever increasing device counts and clock rates. There are several approaches to reducing the power. In this work clock gating technique is applied to ALU to optimize the power. With the conventional type of arithmetic and logic unit that executes all the operations at the same time, the power dissipation gets uncontrolled.

In clock gating technique function has one dedicated module. When one instruction executes in their respective module, others module that was not used by current executing instruction must gated off by the clock gate.

ALU is tested for different load conditions and supply voltages. It is found that it consumes a power of only 23.285W @15MHz with a maximum frequency of 281.770MHz at a supply voltage of 2.4V under load current of 4.8mA. This clock gating technique can be extended to whole system to achieve more power saving. One of the main challenges in future Processor design will center on devising new circuit techniques that help lower power without impacting overall circuit performance.

9. FUTURE SCOPE:

Using Clock gating we can reduce the dynamic power consumed. We must be able to reduce leakage power. Latest FPGA techniques are based on 28 nm technology which contributes certain leakage power. So, there is need to reduce this leakage dynamic power along with dynamic power.

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