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FPGA Improved I2C Protocol for Multiple Slave Device Using VHDL

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Abstract: *In this, slave devices that are interfaced with the FPGA (Working as the I2C master device) are RTC device, EEPROM device and an OV7620 image sensor device. The work flow goes from specification of the complete system to functional design using VHDL language. Design verification with simulated waveform results are presented in the thesis. Hardware verification is also done and practical results are presented. Multiple device interfaces on the same I2C bus with efficient architecture implementation is done and results are compared with the reference work done in the filed earlier.*

Key Words: *I2C protocol, communication, transmit 8-bit,Inter Integrated Circuit, EEPROM, SCL and SDAetc.*

1. INTRODUCTION:

An embedded system physical size get reduce by reducing the size of transistor. Philips Electronics design the protocol to overcome all these problems in the communication between different Integrated IC called Inter IC protocol.I2C protocol is used by different devices such as keyboard, memory, cell phone ,TV, etc. Physically I2C bus consists of two wires SCL and SDA. These are active high, bidirectional and half duplex in nature. I2C is multi master bus it means that more than One IC is capable for data transpiring . All the device associated with SCL and SDA line having interesting location. Any gadgets go about as transmitter or beneficiary relying upon the idea of the gadget. Here master initiate the data transfer and data get exchange between master and slave. SCL line controls all the communication between master and slave. By utilizing clock extending SCL and SDA line evade collision.SCL and SDA line are bidirectional lines. Today consumers demands more functionality, speed, energy efficient and power optimized device. A system consists of a set of components that provide a useful behaviour or service. Power dissipated on clock lines in a logic chip is approximately 30-50%. Clock signals have been an incredible wellspring of force scattering in light of high recurrence and burden. Clock signals don't play out any calculation and principally utilized for synchronization. Subsequently these signs are not conveying any data.

Gated-clock is quite possibly the main methods to decrease power dissipation. By the gated-clock method, power dispersed on clock lines including simultaneous capacity components, for example, flip-slumps and hooks can be saved by stopping the clock of devices when there is no function required. To increase the speed, we have studied two communication protocols SPI & I 2C. Both SPI and I2C offer great help for correspondence with lowspeed device, however SPI is more qualified to applications in which gadgets move information streams, though I2C is better at multi-ace "register access" applications. Transmitting and receiving the information between two or more than two devices require a communication path called as a bus system. A I2C bus is a bidirectional two-wired serial bus which is used to transport the data between integrated circuits. The I2C stands for “Inter Integrated Circuit”. It was first presented by the Philips semiconductors in 1982. The I2C transport comprises of three information move paces, for example, standard, quick mode and high speed data. The I2C bus supports 7-bit and 10-bit address space device and its operation differ with low voltages.

The I2C is a sequential transport convention comprising of two sign lines, for example, SCL and SDL lines which are utilized to speak with the device. The SCL represents a 'sequential clock line' and this sign is constantly determined by the 'ace gadget'. The SDL represents the 'sequential information line', and this sign is driven by either the expert or the I2C peripherals. Both these SCL and SDL lines are in open-channel state when there is no exchange between I2C peripherals.

2. LITERATURE REVIEW:

Bagdalkar, P. et.al. [2020], *"Hardware Implementation of I2C Controller on FPGA and Validation Through Interfacing with Low-Cost ADC."* In this research work researcher proposed working of the I2C controller is validated through SCL and SDA signals on the oscilloscopeI2C signal analyzer and the real-time ADC sensed signals are transferred to host pc for monitoring in the Simulink through RS232 port. In spite of the robust data processing capability of FPGA it lacks data acquisition interface on-board. One of the peripherals that are missing on the FPGA is analog to digital converter, this paper presents an efficient solution through interfacing a very low cost PCF8591 ADC with FPGA. The two parameters which define the performance of ADC are sampling precision N and sampling rate fs the PCF8591 is 8-bit ADC with maximum conversion rate defined by the maximum speed of the I2C bus which is limited to 100 kHz as the I2C module presents on-chip of PCF8591 supports standard bus mode. These two conditions limit the use of PCF8591 ADC from sensing high-speed signals such as audio signals but at the same time make the PCF8591 ADC most suitable for sensing low-speed signals like current, voltage and power from Hall Effect sensor [1].

Bagdalkar, P. et.al. [2019], *"Interfacing of light sensor with FPGA using I2C bus."* In this research work researcher proposed a PROFIBUS peripheral device that can provide interface to CPU/MCU The executed circuit fulfills the superior prerequisites of hardware for industrial organizations, as per IEC 61158-2. The circuit comprises of Manchester encoder/decoder, time-basic equipment clocks and different capacities important to actualize the information interface layer for mechanical organizations utilizing PROFIBUS-PA conventions. The correspondence between the CPU/MPU and the proposed gadget is directed on I2C sequential correspondence standard. This paper describes the protocols used to read/write commands and data on the device. The circuit was validated on FPGA and can be used as an alternative to commercial models that work with the old parallel ports that are leaving the market [2].

Thiago P. Mussolini et.al. [2019], *"In this reseach work.* This work proposes a PROFIBUS fringe gadget that can give interface to CPU/MCU. The actualized circuit fulfills the superior prerequisites of gear for modern organizations, as indicated by IEC 61158-2. The circuit comprises of Manchester encoder/decoder, time-basic equipment clocks and different capacities important to execute the information connect layer for mechanical organizations utilizing PROFIBUS-PA conventions. The correspondence between the CPU/MPU and the proposed gadget is directed on I 2 C sequential correspondence standard. This paper describes the protocols used to read/write commands and data on the device. The circuit was approved on FPGA and can be utilized as an option in contrast to business models that work with the old equal ports that are leaving the market[3].

Rupal G. et.al. [2018],*.In this research work* This research work proposed exhibits how different interfaces are utilized to transmit and receives information to and from the on-board computers and FPGA. So, any lowspeed of the peripheral devices in the satellite can be interfaced by means of I2C and MIL-STD-1553 protocols. The outcome shows the least utilization of resources. The above-discussed methods for interfacing the system can be utilized in satellites. The satellites require this interfacing between the systems or on-board computers. The chip design of the I2C protocol for AIS receiver is done successfully using VHDL programming in Xilinx ISE 14.2 and verified on Vertex 5 FPGA for pre synthesis. The Model sum simulation waveform depicts the successful data transfer in transmitter end to receiver end. These methods are particularly made us here to Interface S-AIS receiver and on board computers[4].

Deepika et.al. [2018], "*Design of dual master I2C bus controller and interfacing it with DC motor."* In this research works simulation results of the dual master design agree well with the expected or desired I2C bus controller behavior. After one of the master gains control of the bus, it performs the desired function and exhibits behavior which agrees well with the I2C specification. The interfacing of master (FPGA) and the slave device i.e. DC motor also shows the expected behavior and shows how this design works on a physical device. Both the software and hardware part of the design has been successfully implemented. The device utilization on the FPGA was also efficient but it can be further be optimized in the future designs. This project deals with the extension of a single master I2C bus controller to a dual master design i.e. two masters have been able to control the bus. This approach can further be extended to more than two masters and they try to access the bus. The decision logic can be chosen in multiple ways depending on the requirement of the designer. In the future, this design can be made much more beneficial and automated by using logic in which depending on the internal conditions of the protocol, one master wins and others lose the arbitration process [5].

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3. PROPOSED I2C PROTOCOL:

Design Entity

I2C communication protocol at the master device side needed to be implemented using the VHDL. The timing diagram described in the I2C master end we needs change in the physical voltage stage of the SDA signal in reference to the SCLK signal. As for the new approach we are interfacing more than one slave device simultaneously through the same FPGA master device, the entity of the new master device will be modified along with the needed data to be send over the I2C line. Below figure shows the proposed entity of the design.

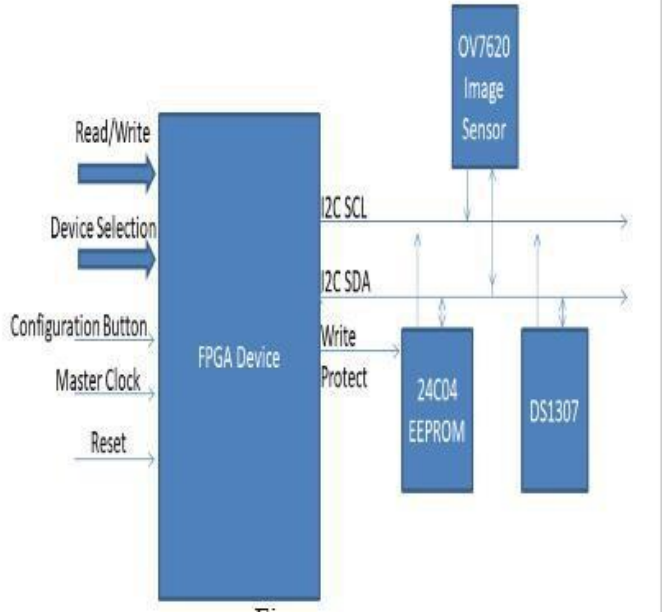

Fig. 1

The master device used over here is XILINX FPGA from SPARTAN6 family. Input given to the FPGA master either using tact switches or sliding switches. Main inputs are the Read/Write button to decide whether the master will write to the communicating device or read from the communicating device. It's a single bit input with following circuit.

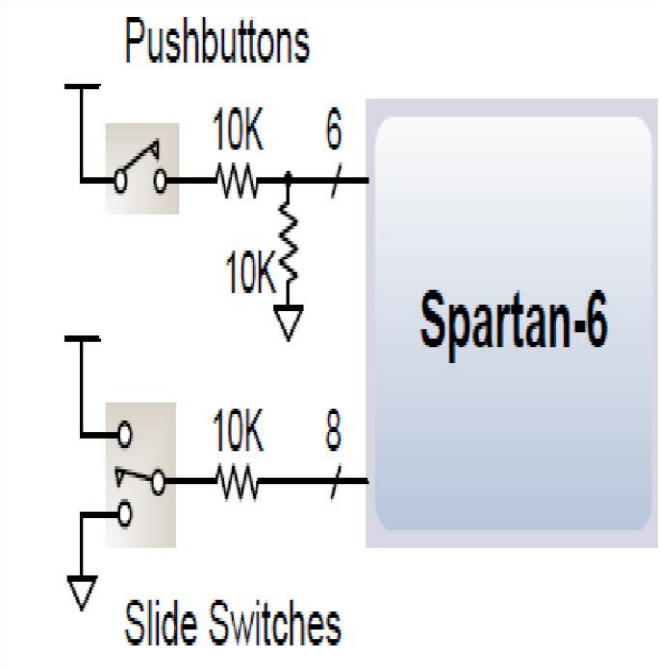

Fig. 2

Similarly slide switches are used to select the targeted slave device among the there. Configuration switch needed to send the register values to write them on the slave devices if needed. And the last reset button to reset the complete device to start from the scratch of the encoded function.

Main clock given to the FPGA device is given from a oscillator source as shown in the below schematic.

4. SIMULATION AND RESULT:

Device Selection for communicating with the I2C Master Bus Controller on FPGA with Arbitration and 10 bit Addressing Scheme

For the multi device communication of the I2C master controller firstly the device had to be selected and for the purpose to show the working of design we had simulated the synthesized design using the integrated simulation software in XILINX. Further implemented the different read and write operations on various devices by selecting their respective read-write addresses. Figure 3. shows the VHDL coded Model Sim output of device selection.

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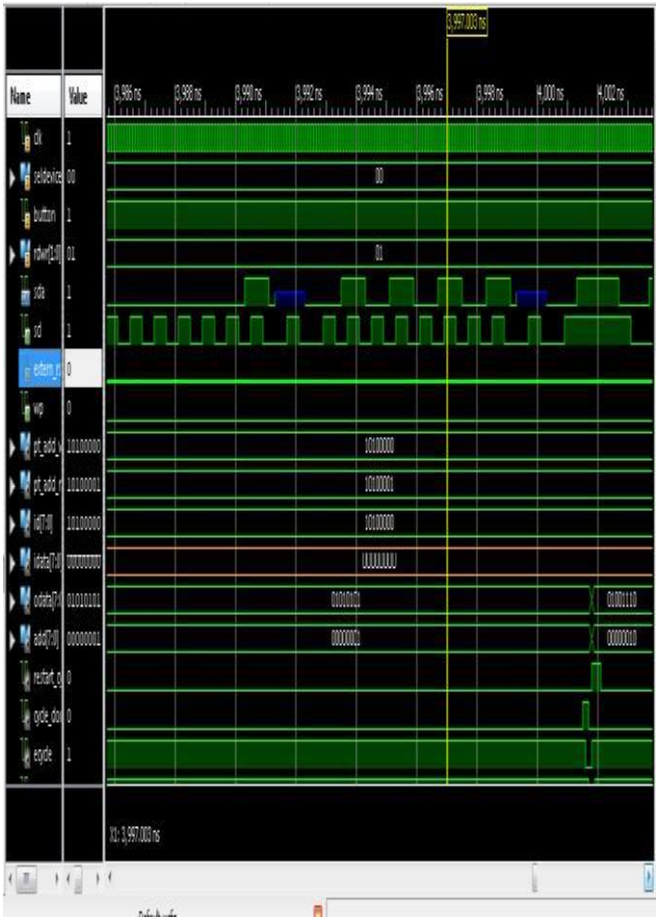

Figure 3: Shows the Device Selection (EEPROM) with write operation

All Xilinx Block is a powerful modeling tool that allows digital complex systems to be designed using a block diagram methodology. The System Generator empowers the demonstrating of advanced frameworks, which can be changed into ModelSim climate and zeroed in on a Xilinx FPGA board . Bit stream automatic generation is supported with synthesis tools and implementation in the run ModelSim and the Xilinx environment. The design is checked and tested in both ISE / ModelSim Xilinx and Impact. The system is studied by real-time hardware implementation with Spartan 6 FPGA, image sensor OV7620, 24C04 EEPROM IC and DS1307 RTC device. The simulation results of an investigation and the waveform read and write operation and various choice of the unit is justified by the I2C specifications mentioned in the IEEE documents.

In the below figure 4. shows the OV7620, 24C04 EEPROM IC and DS1307 devices connection on model Sim.

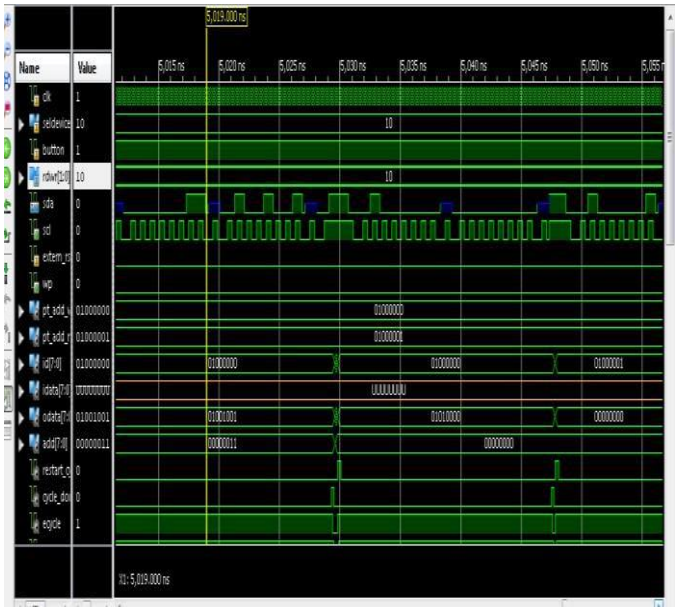

Figure 4: Read Operation with OV7620 device selected

Figure 5.: Shows register address change for write operation on DS1307 IC

Integrated circuits at high-speed Hardware Description Language (VHDL) can be used to model a digital framework at a few degrees of reflection going from the algorithmic level to the gate level with a serious level of multifaceted nature. The simulation results show the successful implementation of multi device interface by the same master only by changing the selection switches to communicate with the respective device is for reading or writing data records in various devices I2C supported.

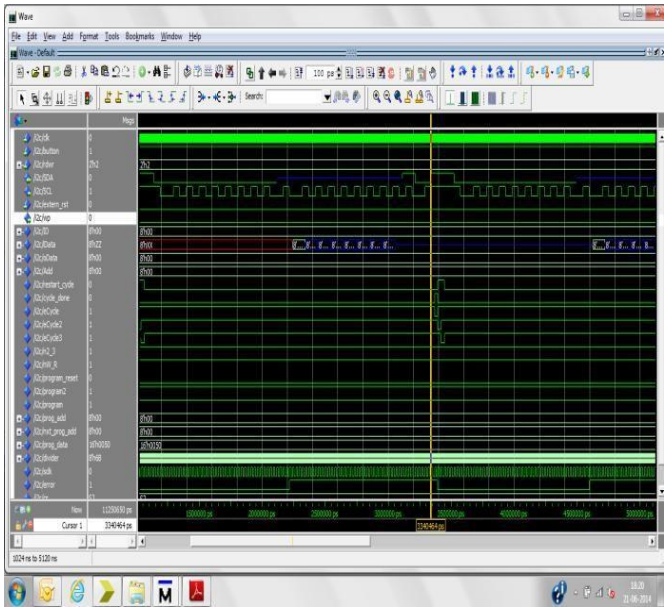

Figure 6. Final output of proposed System on Model Sim

Table -1: component Summary

Logic Utilization	Used	Available	Utilization
No. of Slices	137	54576	0.25%
No. of Slice LUTs	188	27288	0.69%
No. of Fully Used LUT-FF pairs	99	226	43%
No. of bonded IOBs	10	190	5%
No. of BUFG/BUFGCTRLS	2	16	12%

In the below Table 5.2. shows I2C device utilization summary. In this summary shows the number of slices, flip flop, LUTs, IOBs and utilization of these devices. In the above table - 1. shows comparison of device utilization summary, in the above table it can be seen that the proposed I2C method consume significantly a smaller number of devices as compare to other methods.

Table-2: Shows Comparison between Previous Method and Proposed Method

S. No	Result Parameter	Base Paper 2018[5]	Proposed 2021
1	No. of Slices	187	**137**
2	No. of Slice LUTs	350	**188**
3	No. of Fully Used LUT-FF pairs	390	**99**
4	No. of bonded IOBs	52	**10**
5	No. of BUFG/BUFGCTRLS	3	**2**

4. CONCLUSION:

This research work shows an efficient implementation of Multi Device I2C interface using FPGA as Master Device. Research work describes the utility of FSM implementation in HDL coding and also shows the improvement in the architecture formed for the protocol implementation in reconfigurable devices. Multi Device Interface Implementation of I2C Master Bus Controller on FPGA with Arbitration and 10 bit Addressing Scheme. The proposed I2C structure shows better performance as compare to other previous methods. Also reduce the complexity of the proposed method.

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