INTERNATIONAL JOURNAL OF RESEARCH CULTURE SOCIETY ISSN(O): 2456-6683
Monthly Peer-Reviewed, Refereed, Indexed Journal [Impact Factor: 6.834]
Volume - 7, Issue - 9, September- 2023 Publication Date: 30/09/2023

DOIs:10.2017/IJRCS/202309018 --:-- Research Paper / Article / Review

Feasibility Analysis of Wireless Power Transmission for Portable Device by PLL

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Abstract: *This paper mainly proposes a feedback mechanism for detectors PLL single phase by using the phase angle estimated. To control sub system that tracks the phase angle and grid voltage frequency (PLL) phase lock loop is the crucial component. Every algorithm is based on a mixed representation of analog/digital. The proposed system has the capability to eliminate the entirely noise ripple and the line distorted under extreme conditions. It also decreases the setting time of PLL as mathematically up-to 50% the result was analyses with the experimental and simulated are provided for the confirm of the methods valedictory which is proposed.*

Key Words: *Wireless Power Transmission, analog, MATLAB.*

1. INTRODUCTION:

The implementation of Discrete Phase-Locked Loop (PLL) for measurement is a topic of significant interest in the field of electronics and instrumentation. Phase-Locked Loops are widely used in various applications where precise synchronization, frequency tracking, and phase detection are crucial for accurate measurements. In this introduction, we will explore the importance of PLLs in measurement systems, the challenges faced in their implementation, and the objectives of this research. Measurement systems play a vital role in various industries, ranging from telecommunications to scientific research. These systems require accurate and stable frequency references, precise phase detection, and synchronization of signals to ensure reliable and high-quality measurements [1]. Phase-Locked Loops provide an elegant solution to address these requirements, making them an essential component in modern measurement instruments.

The Discrete Phase-Locked Loop is a digital implementation of the classic analog PLL, offering several advantages such as flexibility, ease of implementation, and the ability to perform complex signal processing tasks [2]. Unlike analog PLLs, which are based on continuous-time analog components, the Discrete PLL operates in a digital domain, making it suitable for integration with modern digital systems and signal processing techniques [3].One of the primary objectives of this research is to design and implement a Discrete PLL for measurement applications, taking advantage of the benefits offered by digital signal processing and precise control of digital systems. The discrete nature of the PLL allows for easy integration with digital measurement systems, facilitating seamless communication between different component

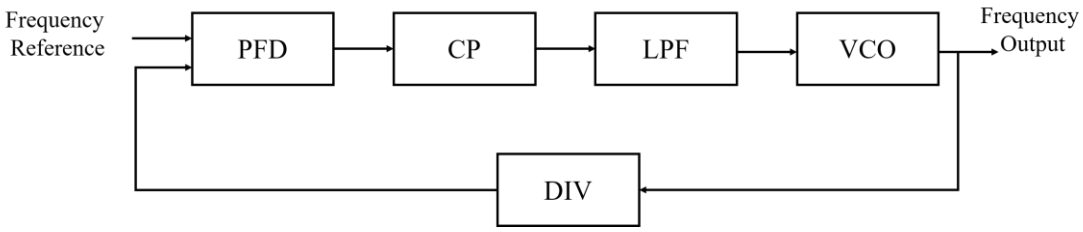

Fig. 1 Schematic of Analog Phase lock loop

2. LAYOUT OF THE SYSTEM:

The layout of the schematic diagram for the phase-locked loop (PLL) simulation is designed to reflect the combination of discrete analog components and behavioral blocks used in the model. The schematic diagram visually represents the components and their connections, allowing users to easily understand the overall structure and functionality of the PLL simulation. The schematic diagram begins with the representation of the charge pump and loop filter, which are modeled using discrete analog components. These components, such as resistors and capacitors, are arranged in a specific configuration to accurately simulate the charge pump and filter operations. Their connections are depicted clearly in the diagram to show how they interact with each other.

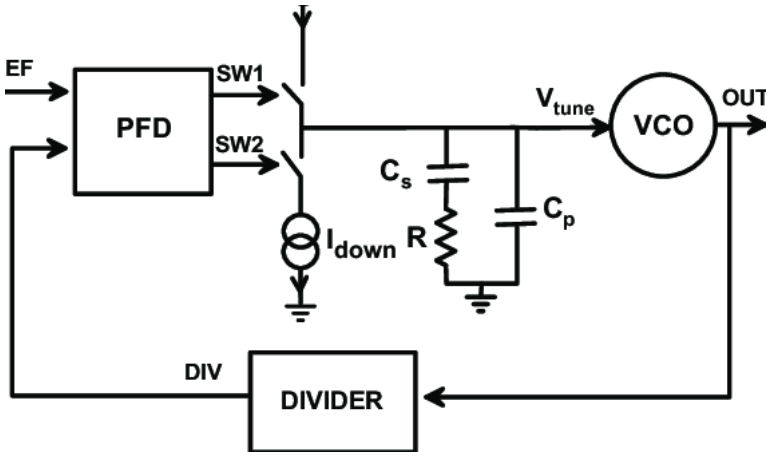

Fig.2 Schematic diagram of PLL

Next, the voltage-controlled oscillator (VCO) is represented using the Simscape™ Electrical™ Voltage-Controlled Oscillator block. This behavioural block simplifies the representation of the VCO's behaviour, and its connection to the charge pump and filter is visually indicated in the schematic diagram. The phase detector is shown using D-type flip-flops in a simplified form using Simulink® blocks. The connections between the D-type flip-flops and other components in the PLL are also illustrated in the schematic diagram.

3. SIMULATION MODEL:

Simulink diagram in MATLAB of Discrete Analog Phase Lock Loop is shown in fig. 3.4, consisting of Main grid connected with Local Generator Unit 1 and Unit 2 feeding the load.

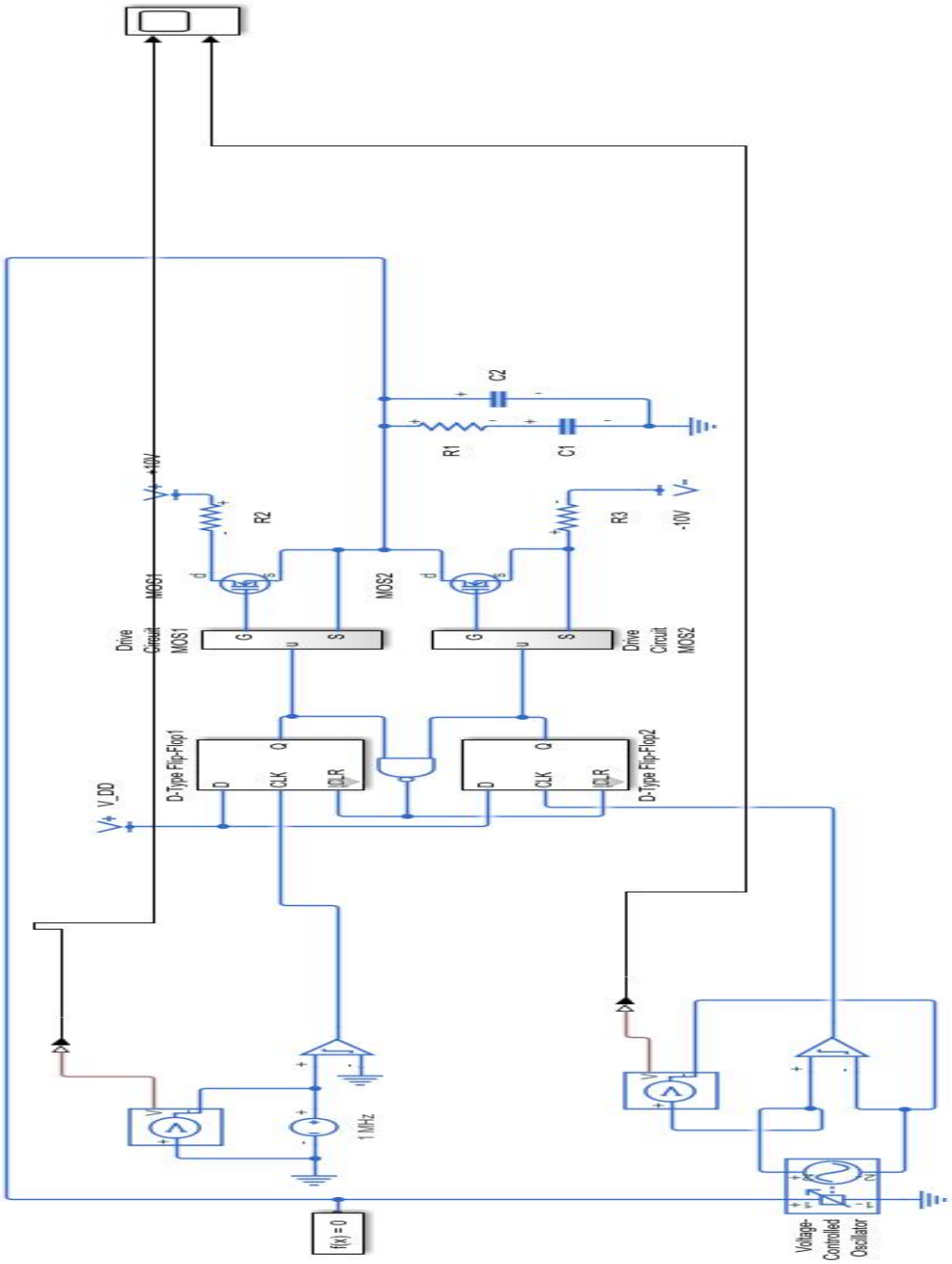

Fig3 Simulink diagram of discreet analog PLL

4. RESULT:

This chapter presents a comprehensive analysis of the performance and effectiveness of the proposed PLL design. This chapter aims to showcase the outcomes obtained from extensive simulations and experimental evaluations, providing insights into the PLL's functionality under various conditions. The discrete analog PLL was designed with meticulous attention to detail, incorporating key components such as the voltage-controlled oscillator (VCO), phase/frequency detector (PFD), loop filter (LF), and charge pump (CP) to create a robust and efficient system.

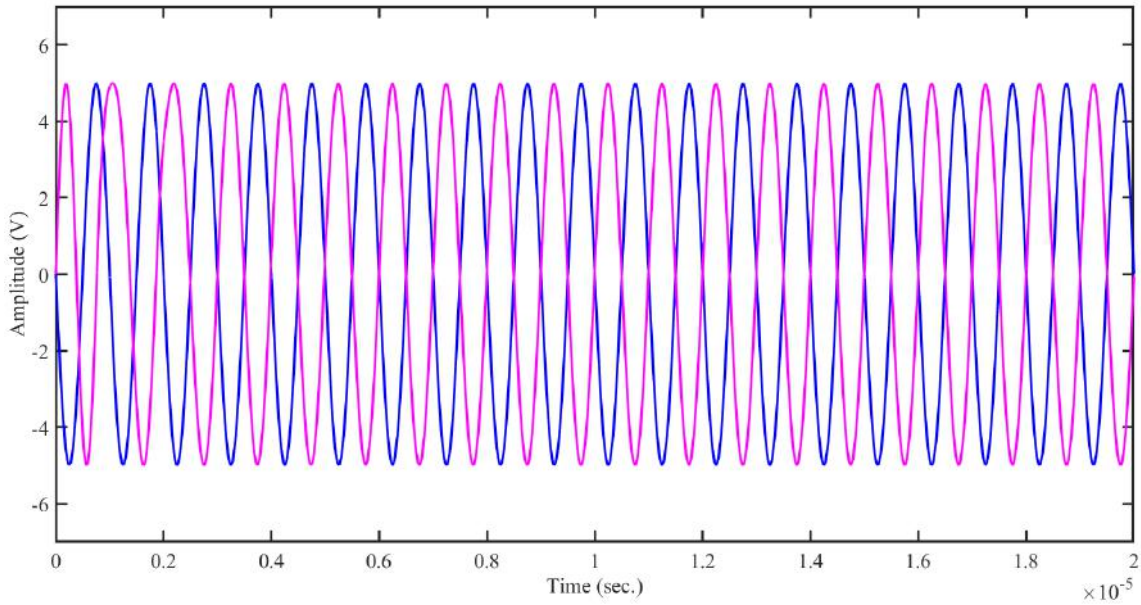

Fig. 5.1 Output wave form not in sync with carrier wave.

REFERENCES:

1. Wang, X., Han, Q., Li, Y. *et al.* Stable frequency transfer for clock synchronization for telecom networks. *EURASIP J. Adv. Signal Process.* 2023, 45 (2023).
2. A, Gothandaraman, "Design and Implementation of an All Digital Phase Locked Loop using a Pulse Output Direct Digital Frequency Synthesizer," *University of Tennessee - Knoxville*, 2014.
3. Sayadi, M., Farshidi, E. A fast locked and low phase noise all-digital phase locked loop based on model predictive control. *Analog IntegrCirc Sig Process* 88, 401–414 (2016).
4. B. Yu, "An Improved Frequency Measurement Method from the Digital PLL Structure for Single-Phase Grid-Connected PV Applications," *Electronics*, vol. 7, no. 8, p. 150, Aug. 2018.
5. F. Jonsson, "Design and Calibration of Integrated PLL Frequency Synthesizers,", KTH - Royal Institute of Technology, 2008.
6. M. Fan, Matthew Clark, Z.C. Feng, "Implementation and stability study of phase-locked-loop nonlinear dynamic measurement systems," Communications in Nonlinear Science and Numerical Simulation, vol. 12, no. 7, 2007.
7. A. Kumar, "Integration of Phasor Measurement and Communication Capability in a Flexible-Combined Heat and Power Converter Testbed," Virginia Tech., 2022.
8. N. Mijat, D. Jurisic and G. S. Moschytz, "Analog Modeling of Fractional-Order Elements: A Classical Circuit Theory Approach," in *IEEE Access*, vol. 9, pp. 110309-110331, 2021.
9. D.I. Crecraft and S. Gergely, "Analog Electronics Circuits, Systems and Signal Processing," Science Direct, 2002.
10. S. Takagi, K. Wada, N. Fujii and T. Yanagisawa, "Novel automatic tuning system using PLL with switched capacitor circuit technique," *IEEE. APCCAS 1998. 1998 IEEE Asia-Pacific Conference on Circuits and Systems. Microelectronics and Integrating Systems. Proceedings (Cat. No.98EX242)*, Chiang Mai, Thailand, 1998.